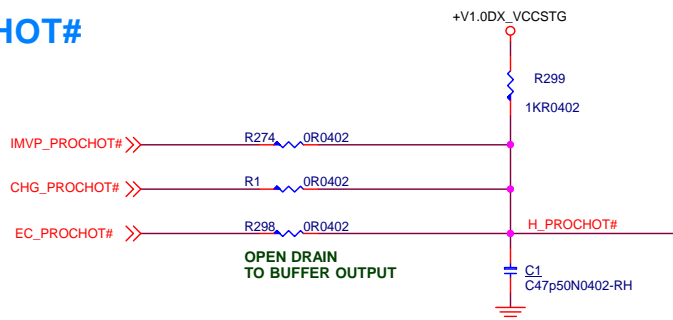
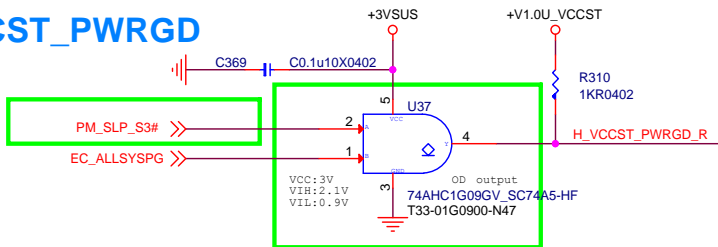


## PROCHOT#



## VCCST\_PWRGD



1782 EVT Add circuit for VCCST\_PWRGD power sequence  
Modify U83 74AHC1G09GV and connect PM\_SLP\_S3# control . page 2. 5/22

### MSR Privacy Bit Feature

CFG3	1 = Debug capability is determined by IA32_Debug_Interface_MSR (0xC80) bit[0] setting 0 = IA32_Debug_Interface_MSR (0xC80) bit[0] default setting overridden
------	---

### eDP Enable

CFG4	1 = Disabled 0 = Enabled
------	-----------------------------

### PEG DEFER TRAINING

CFG7	1: (Default) PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training
------	---

### PCI Express \* Static X16 Lane Numbering Reversal

CFG2	CFG[2]: PCI Express* Static x16 Lane Numbering Reversal. 1 = Normal operation 0 = Lane numbers reversed.
------	--

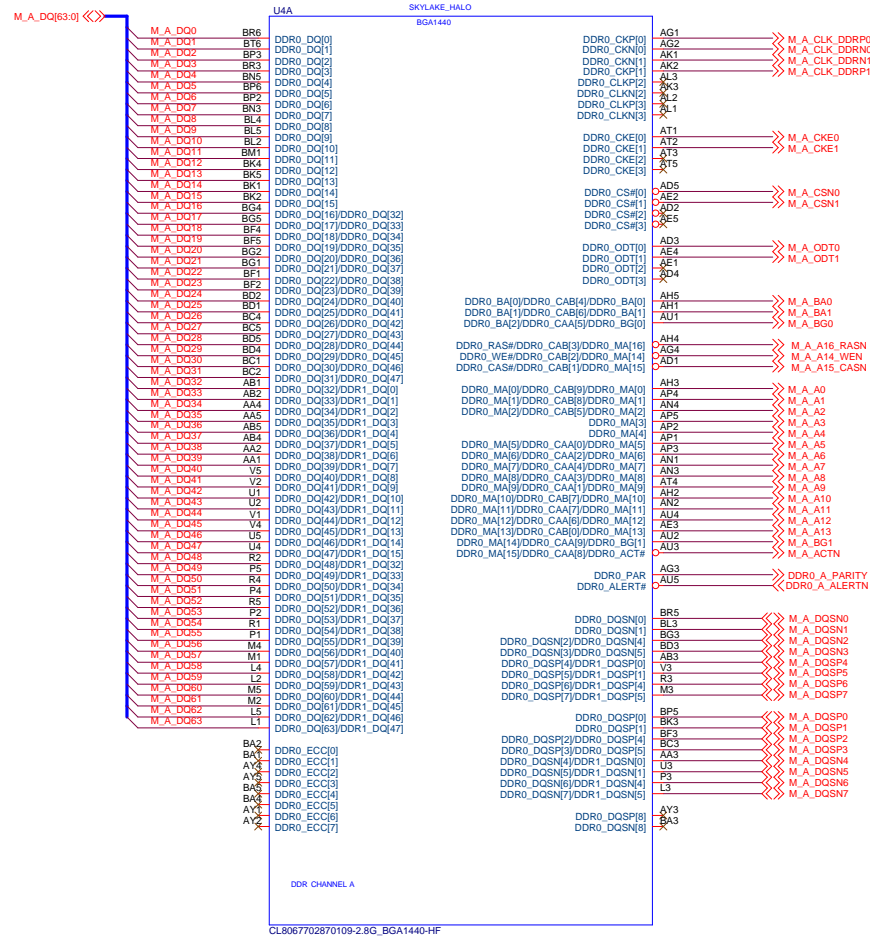
### PCI Express\* Bifurcation

CFG[6:5]	00 = 1 x8, 2 x4 PCI Express* 01 = reserved 10 = 2 x8 PCI Express* 11 = 1 x16 PCI Express*
----------	--

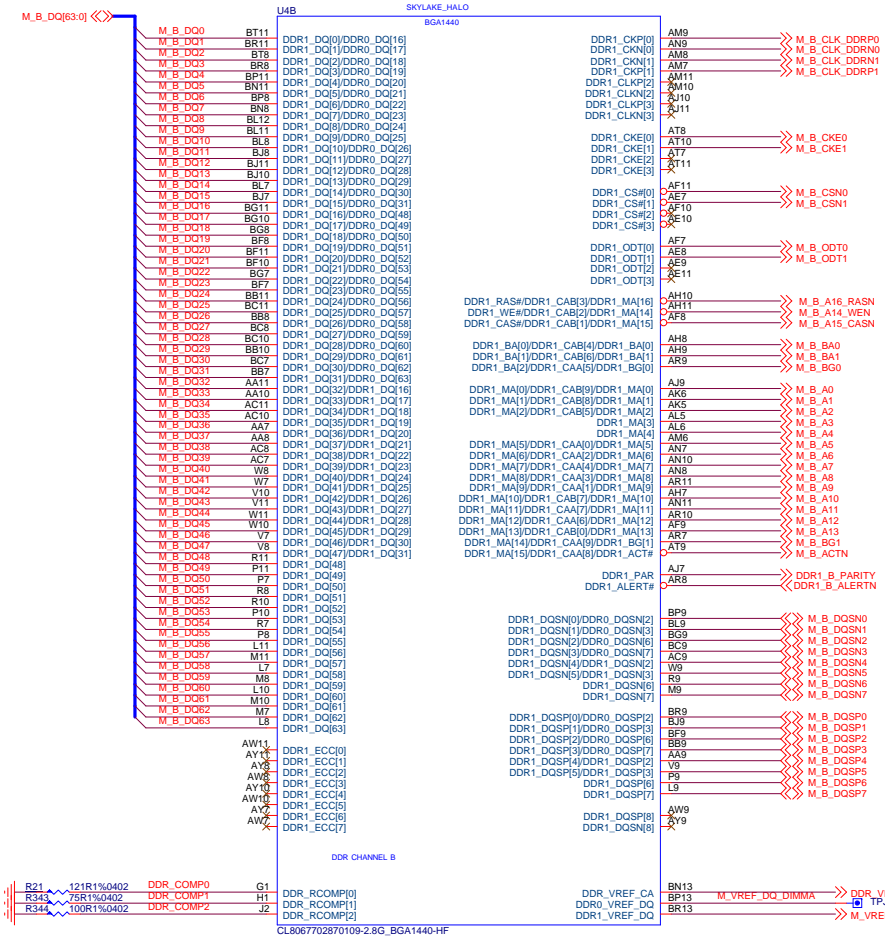
<b>msi</b> MICRO-STAR INT'L CO.,LTD.	
Title <b>Skylake(HOST)</b>	
Size Document Number	Rev
Custom <b>MS-16K41</b>	<b>0A</b>
Date: Friday, November 04, 2016	Sheet 2 of 66



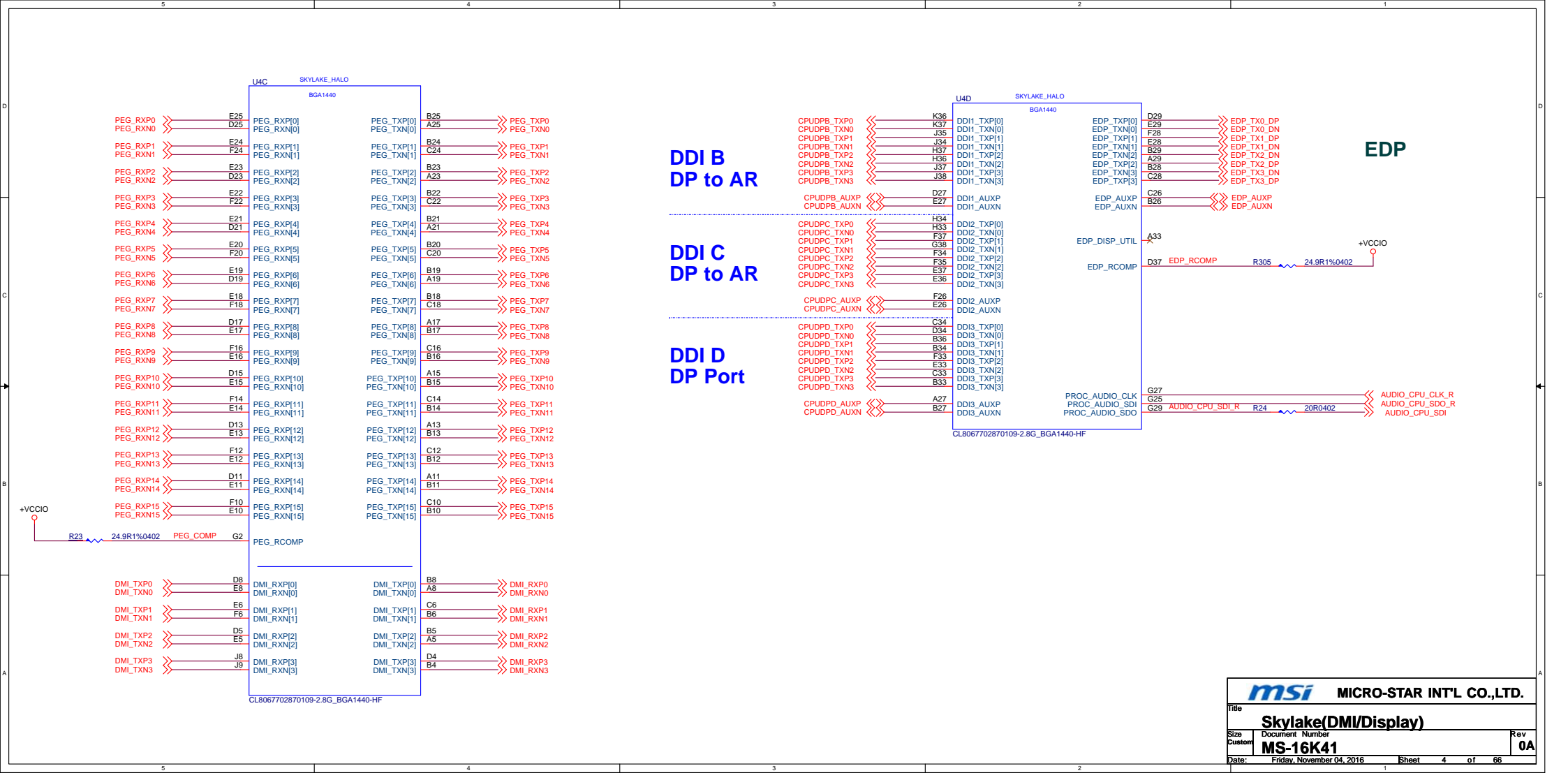
## DDR Channel A



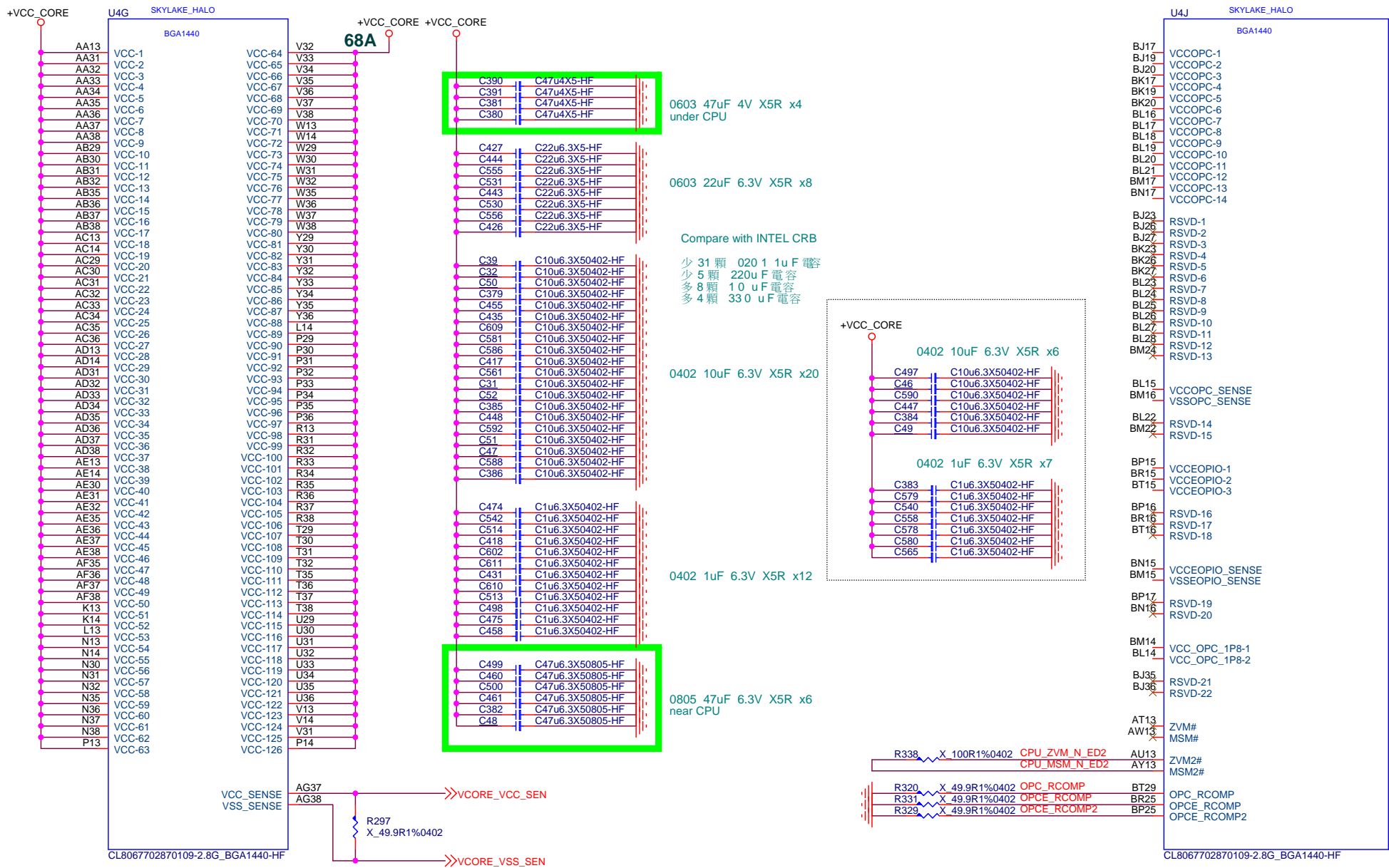
## DDR Channel B



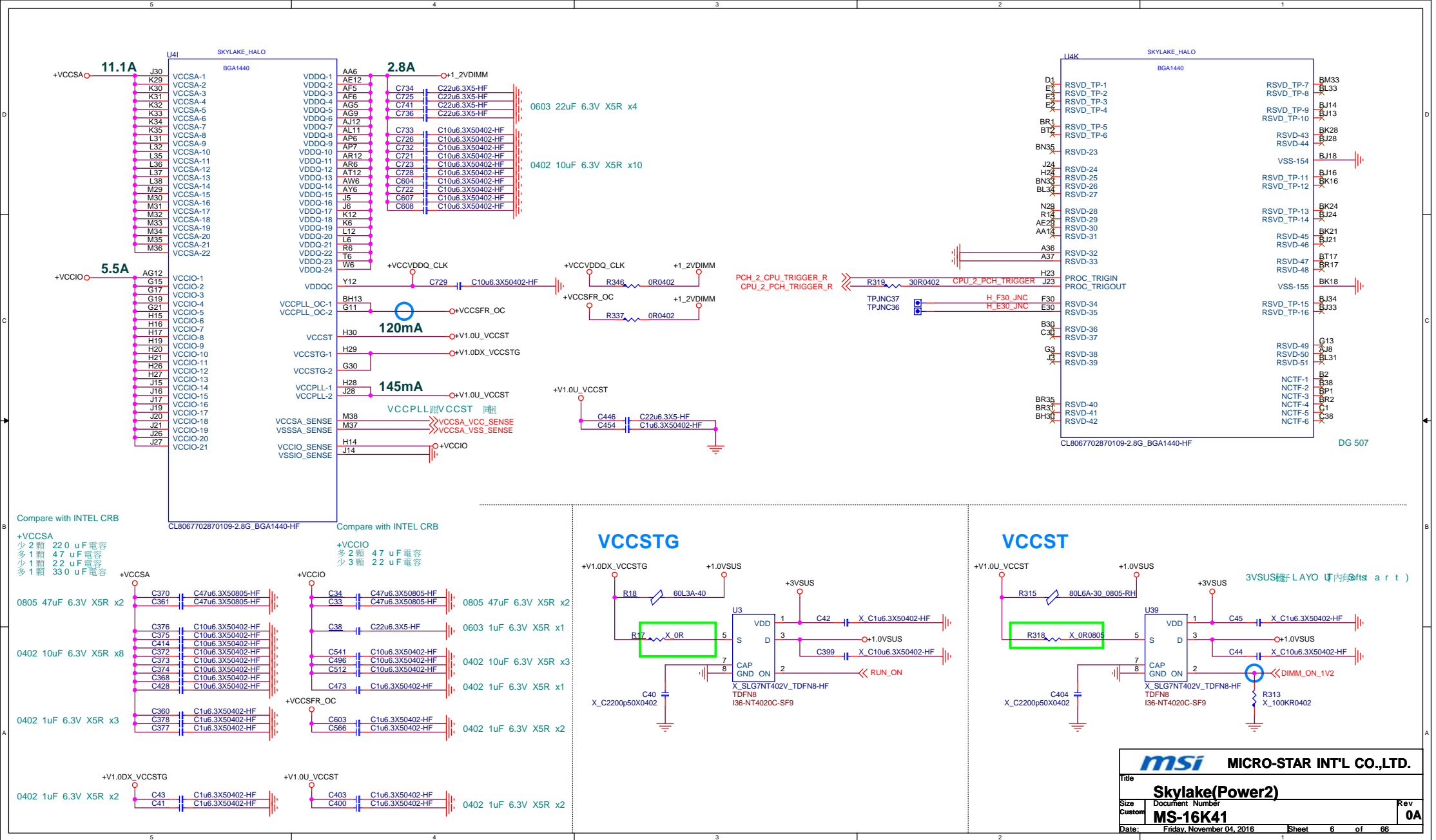














Compare with INTEL CRB

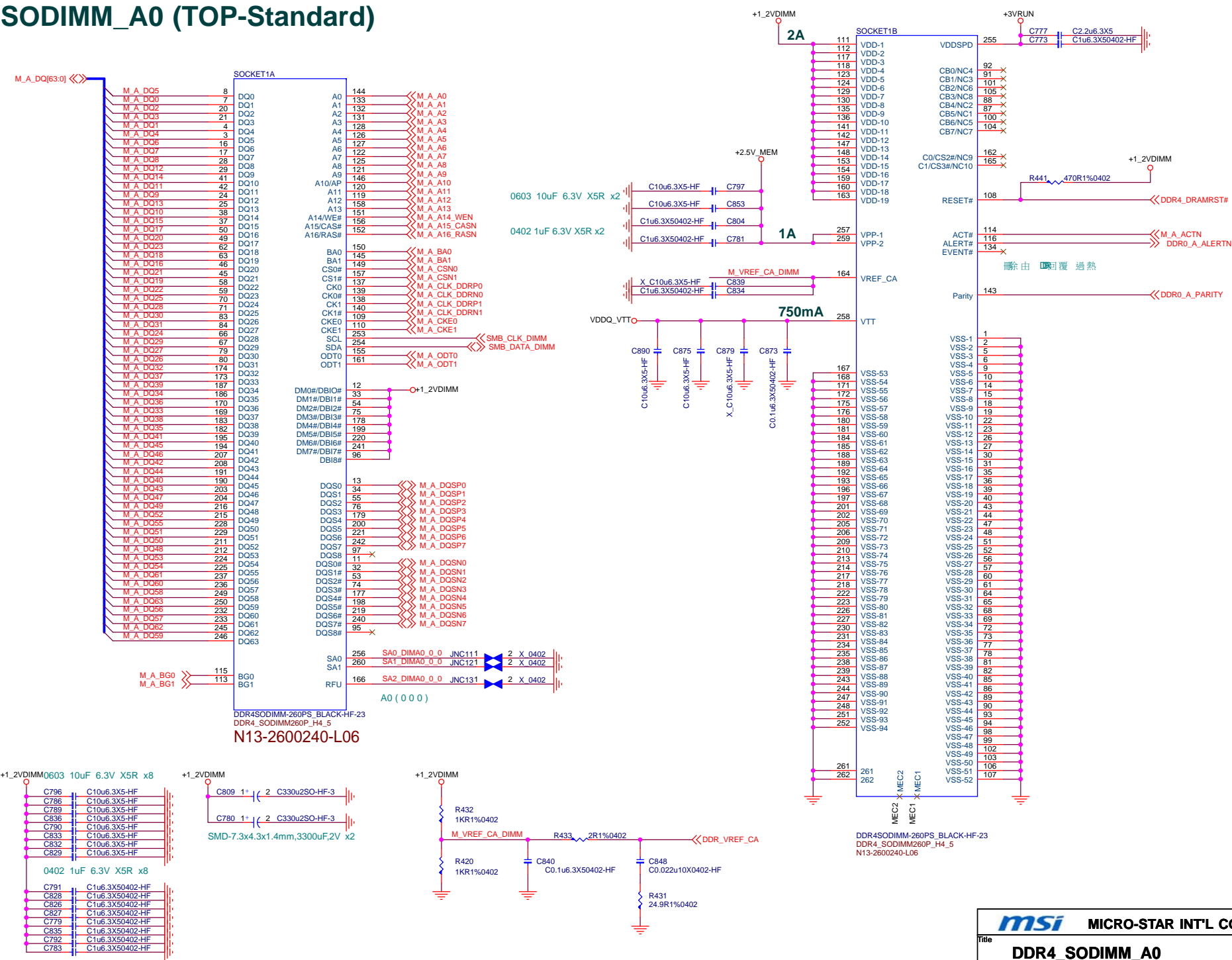
+VCCGT  
少 39 顆 020 1 1uF 電容  
多 7 顆 220uF 電容  
少 17 顆 10 uF 電容  
多 4 顆 33.0 uF 電容

## GT2 55A



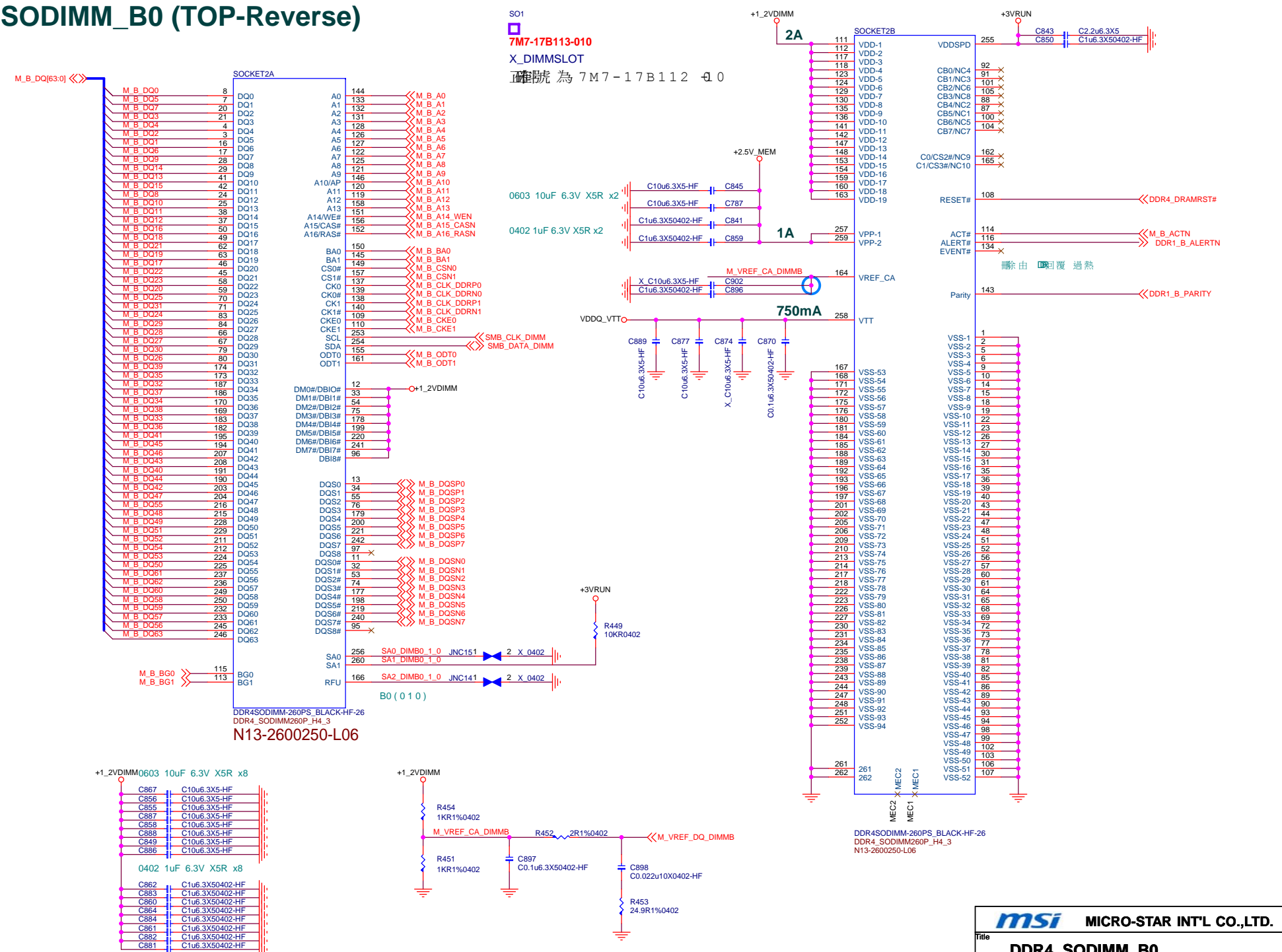


SODIMM\_A0 (TOP-Standard)



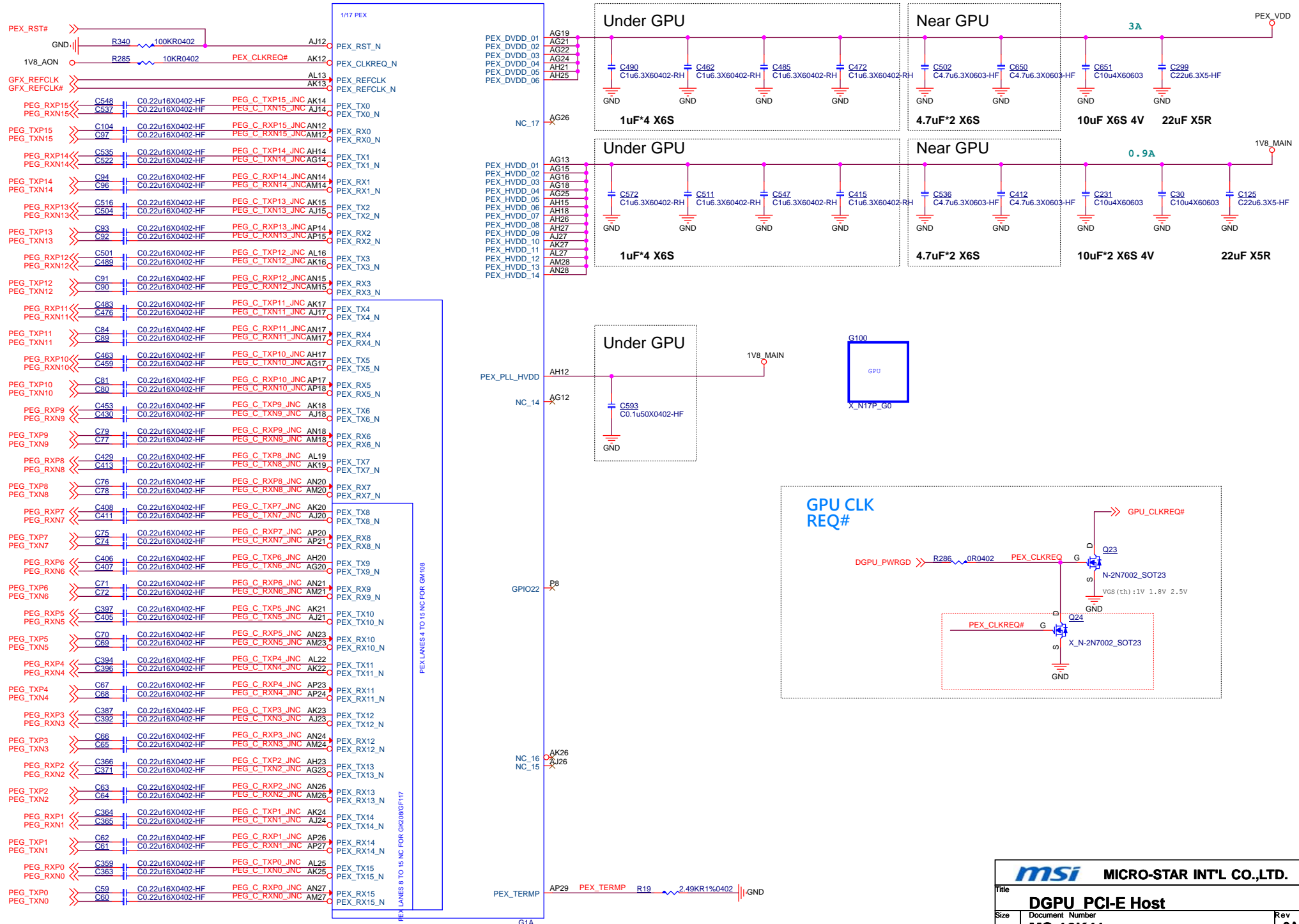


SODIMM\_B0 (TOP-Reverse)



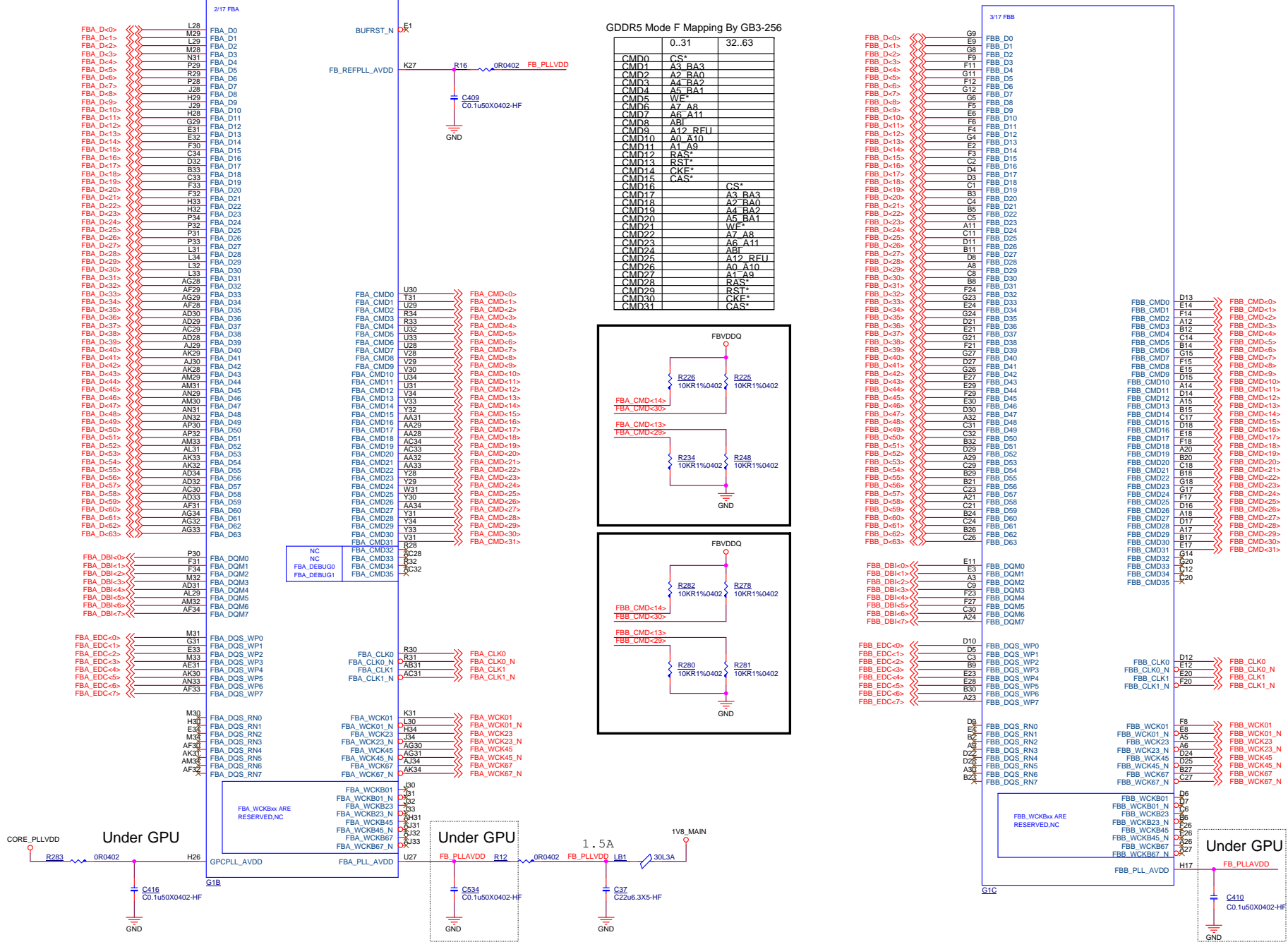


## GPU PCI EXPRESS



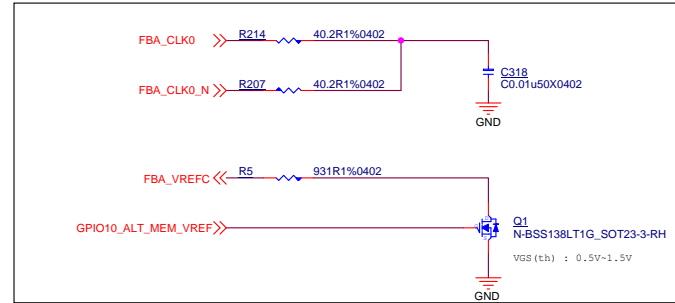
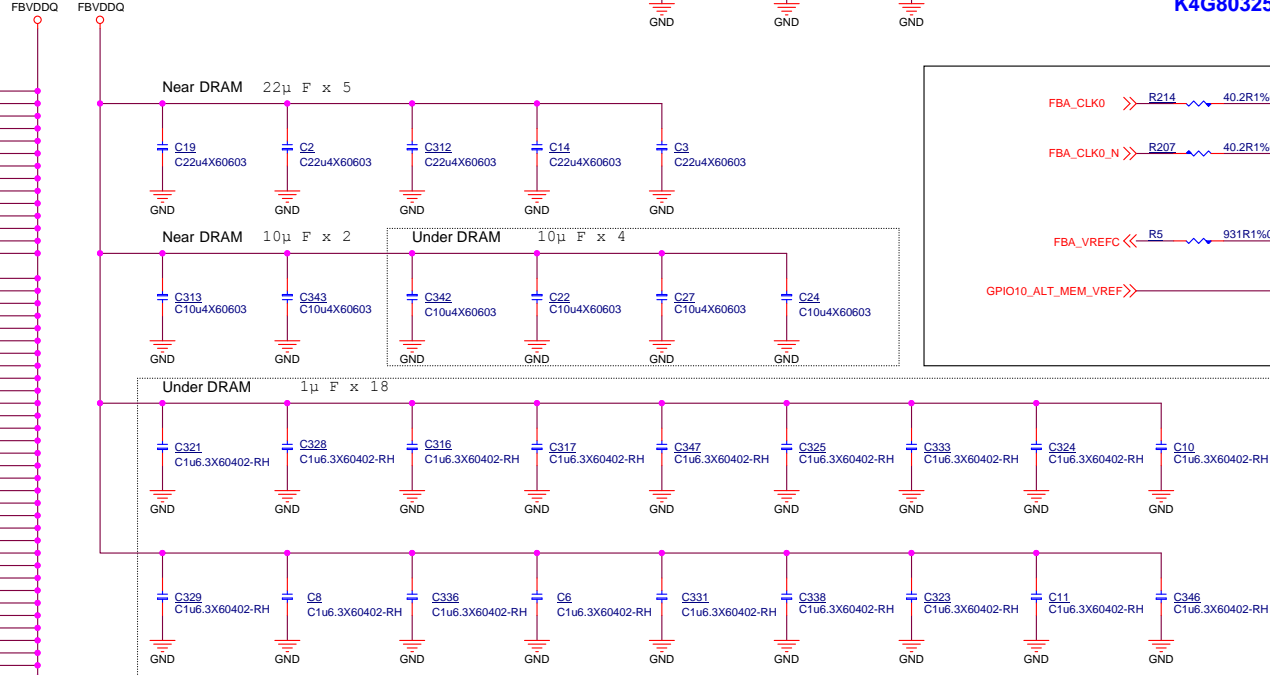
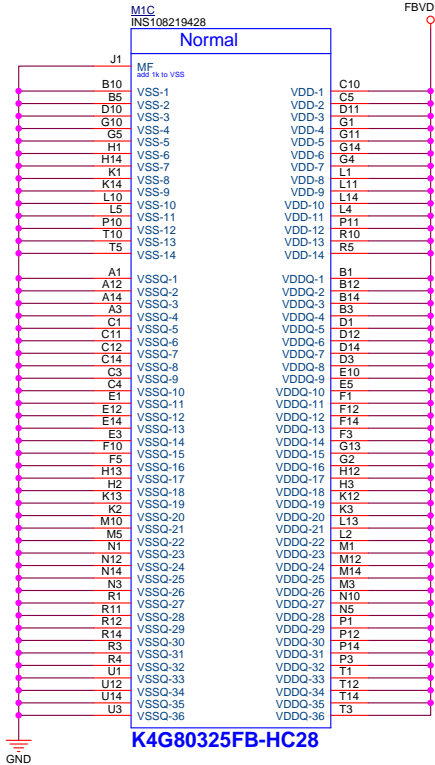
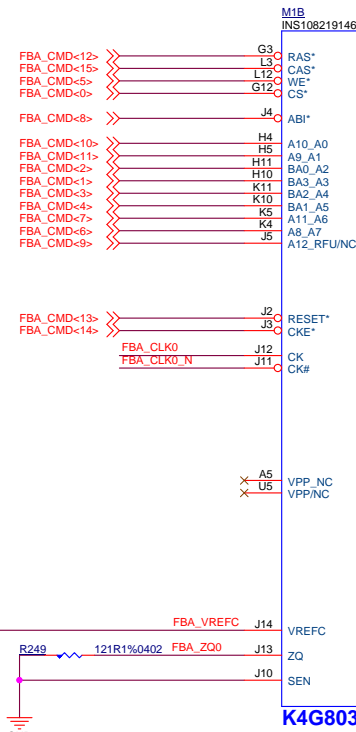
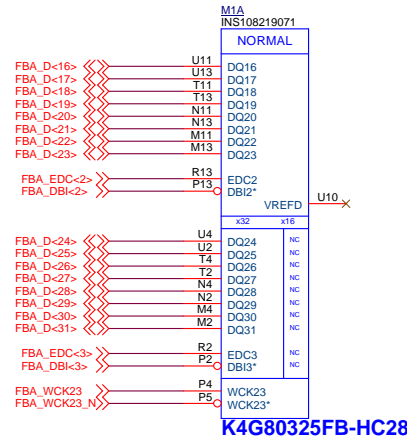
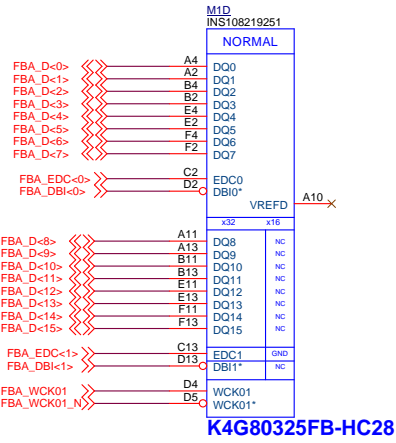


# GPU Frame Buffer Partition A/B



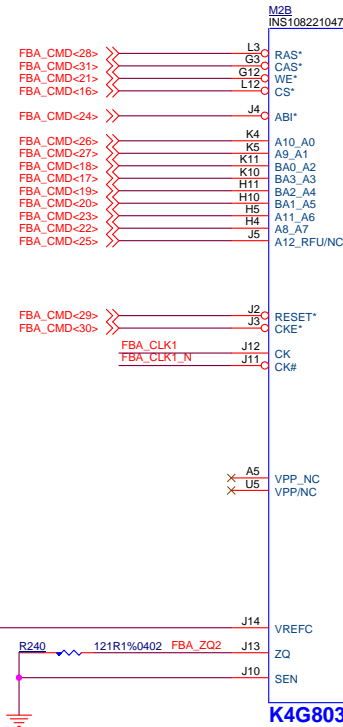
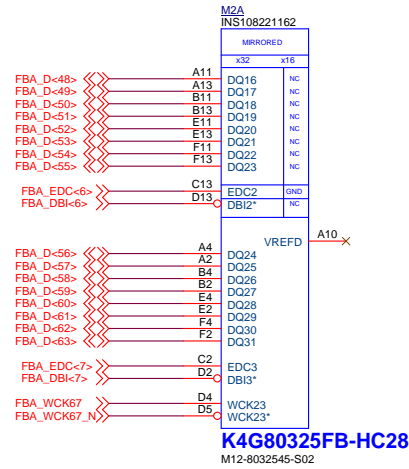
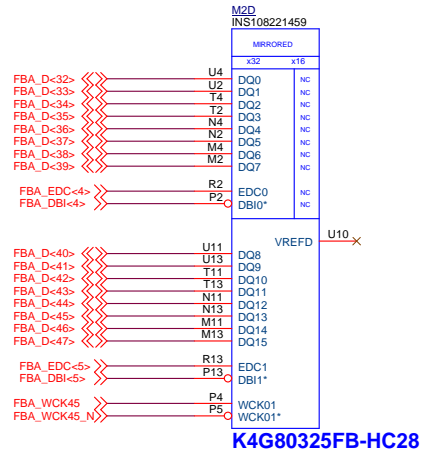


# DGPU\_GDDR5 FrameBuffer A0

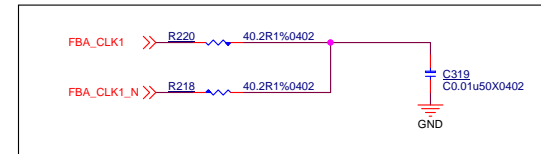
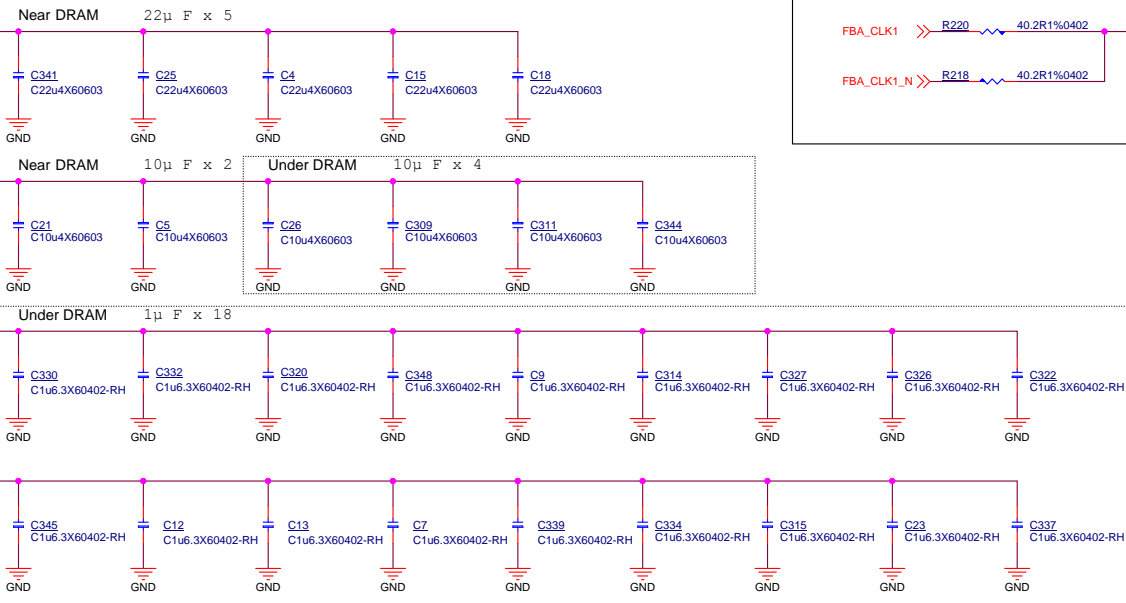
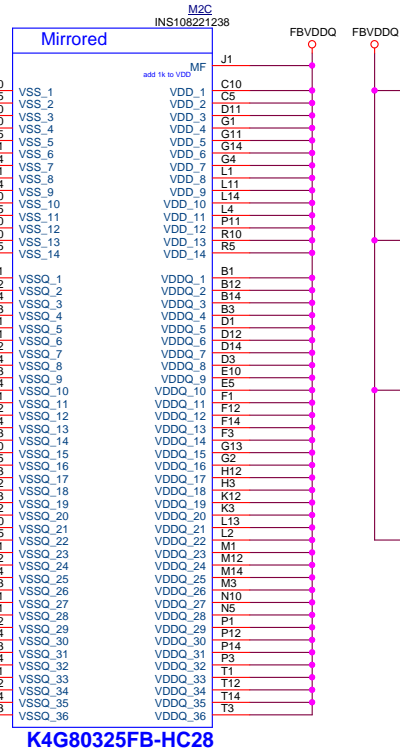




# DGPU\_GDDR5 FrameBuffer A1

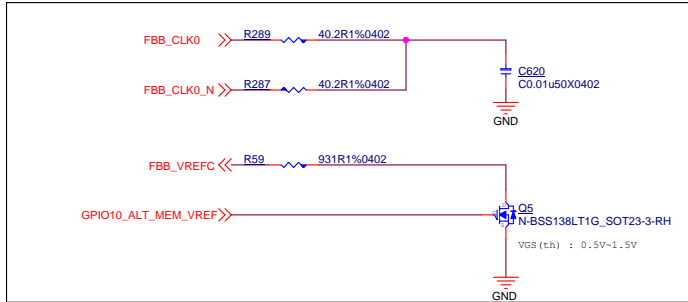
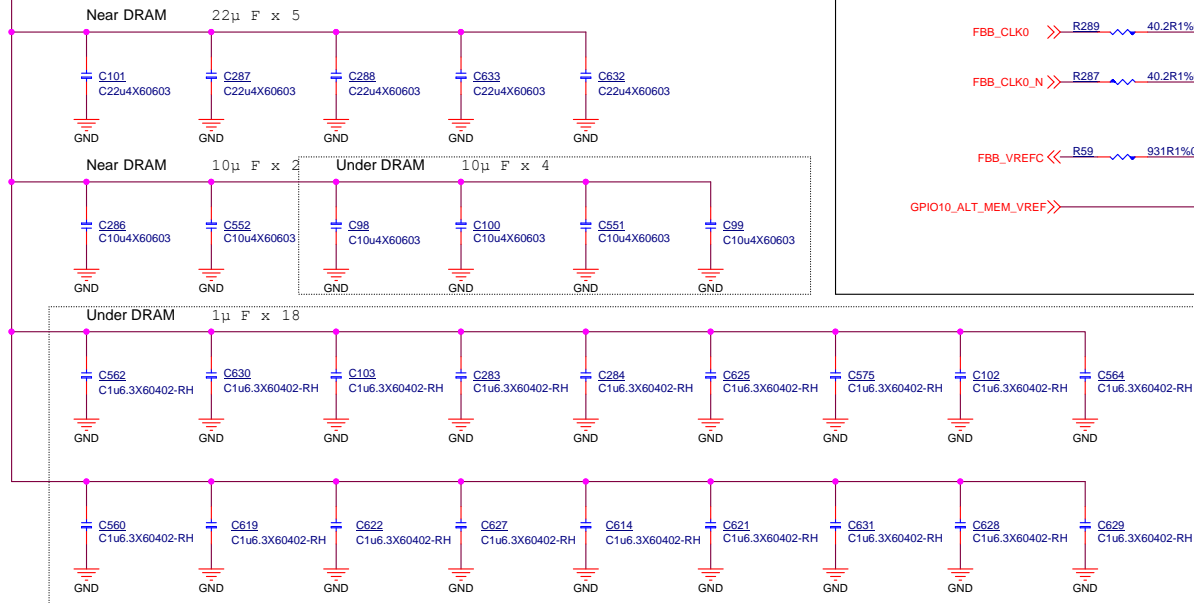
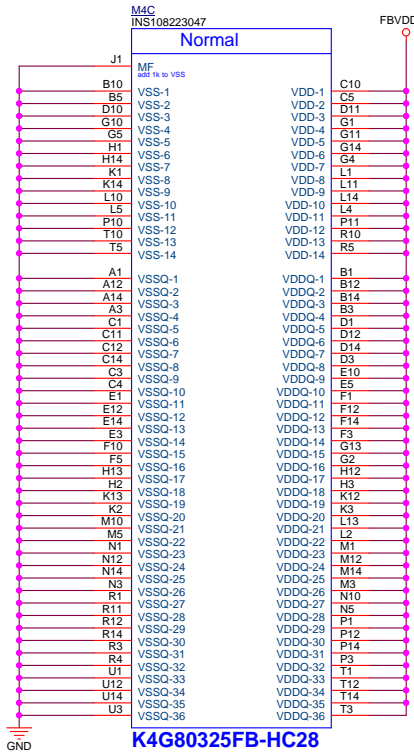
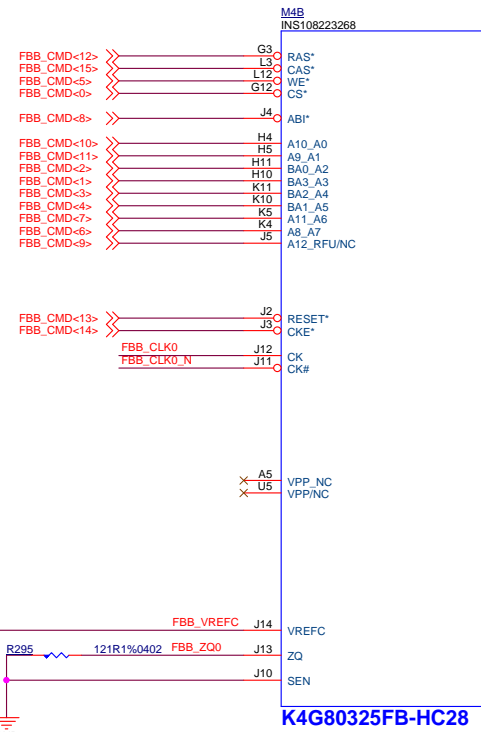
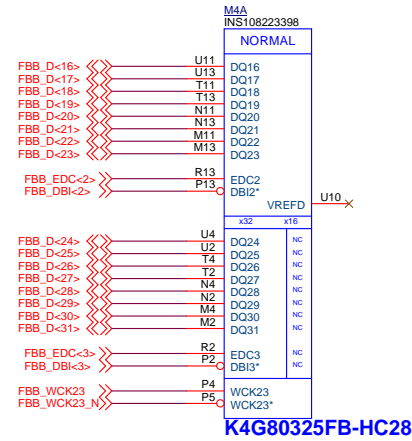
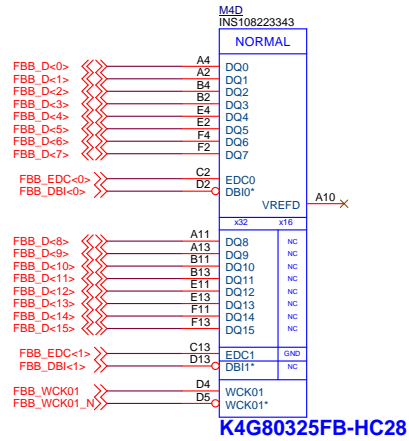


2016/03/23 Remove R14 to follow NV CRB



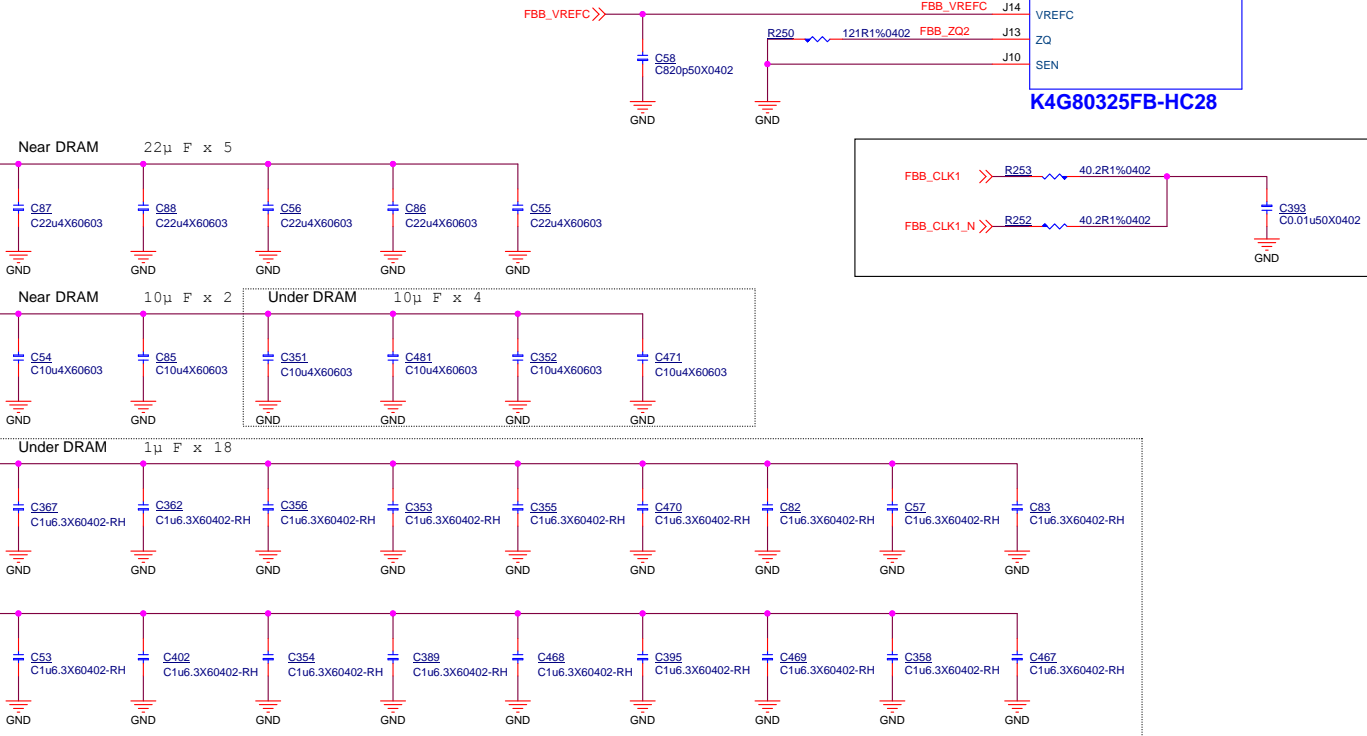
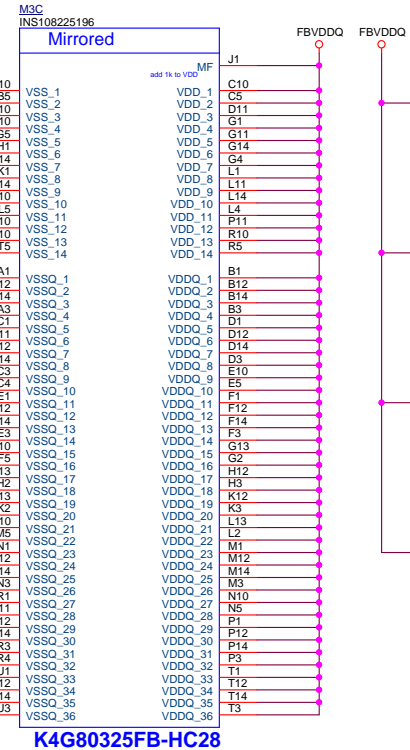
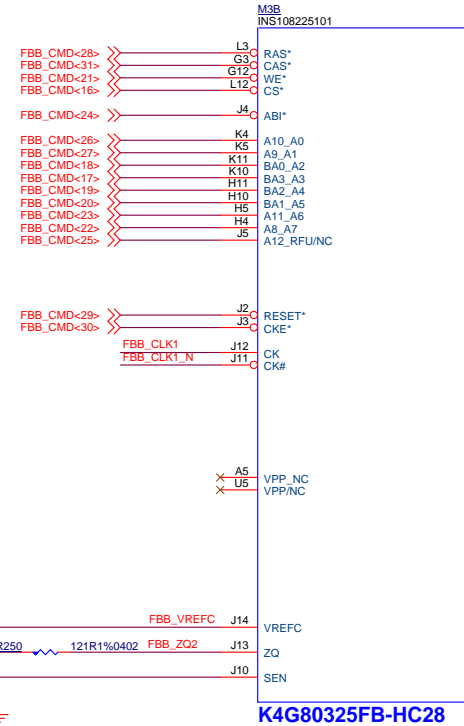
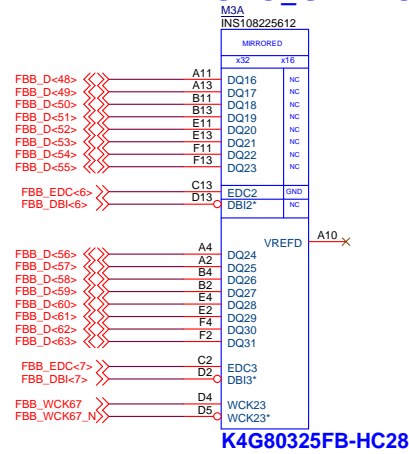
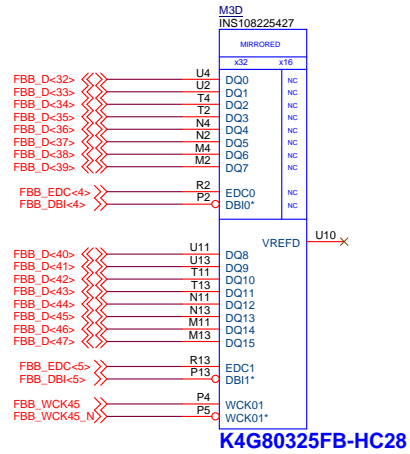


# DGPU\_GDDR5 FrameBuffer B0



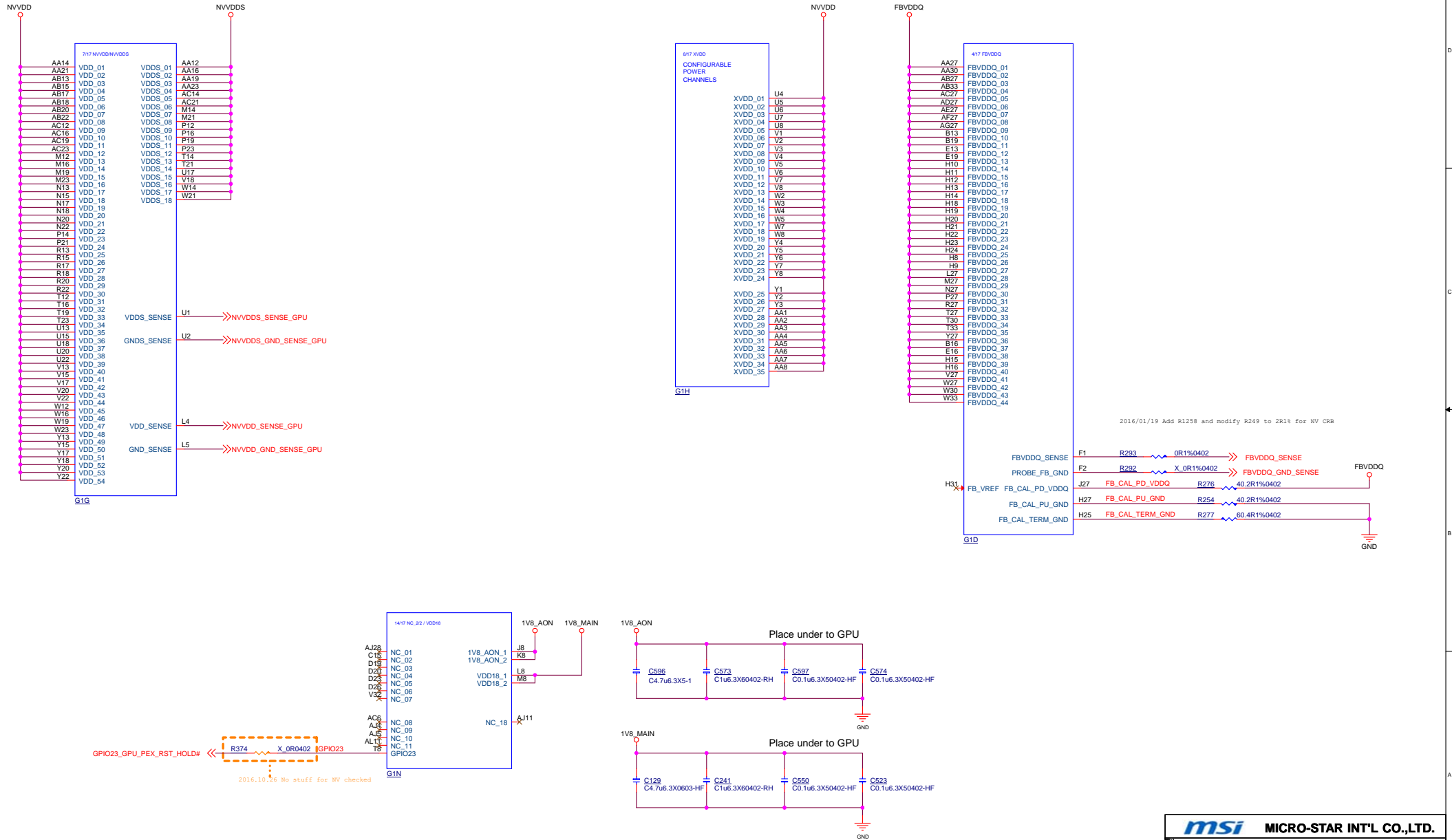


# DGPU\_GDDR5 FrameBuffer B1



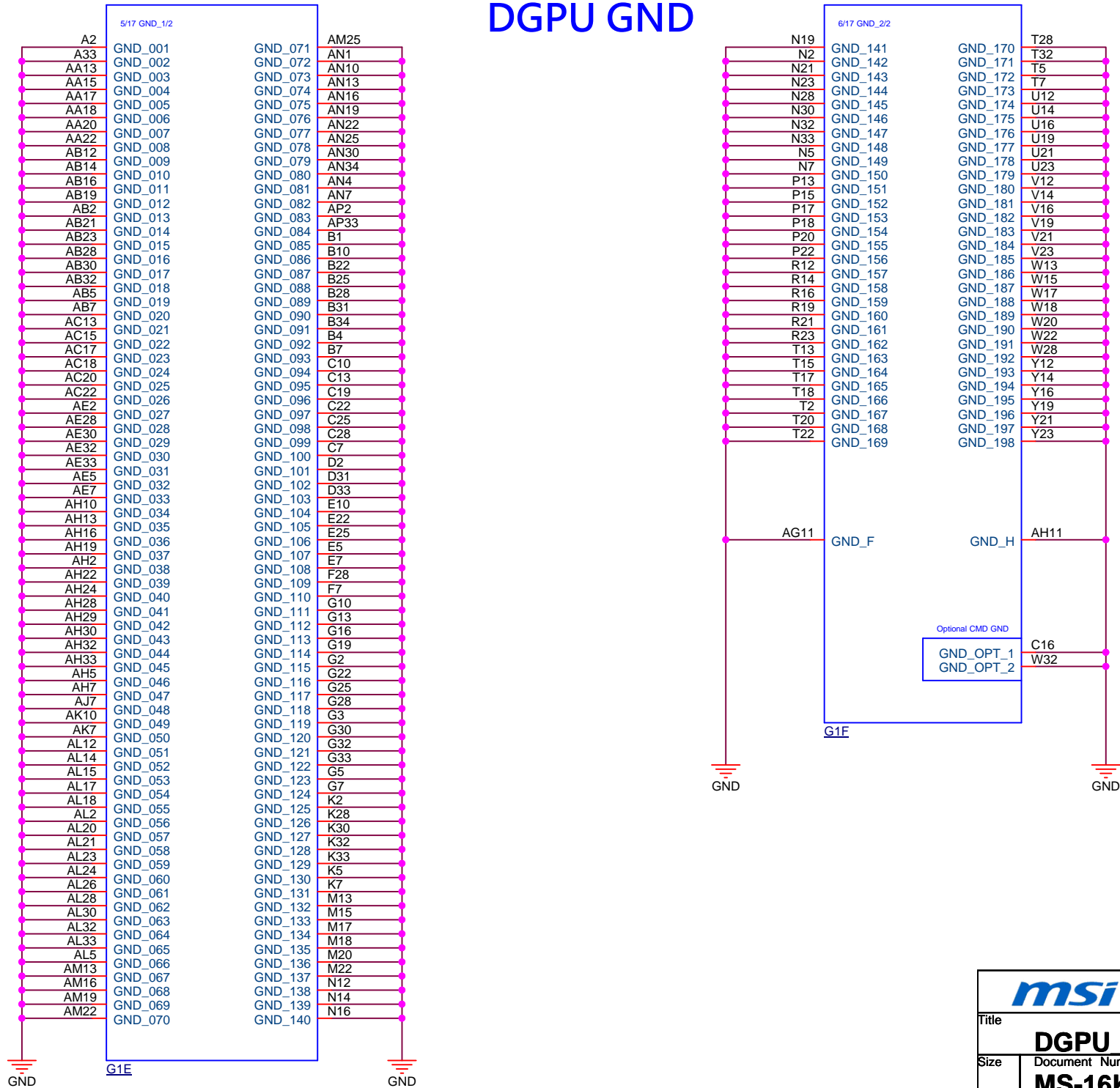


# GPU NVVDD, FBVDDQ



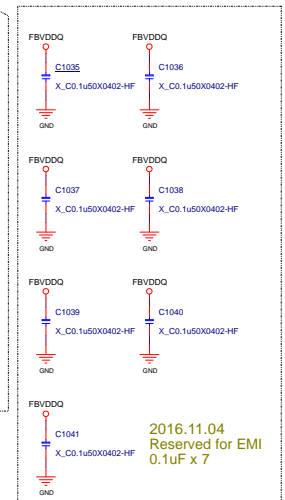
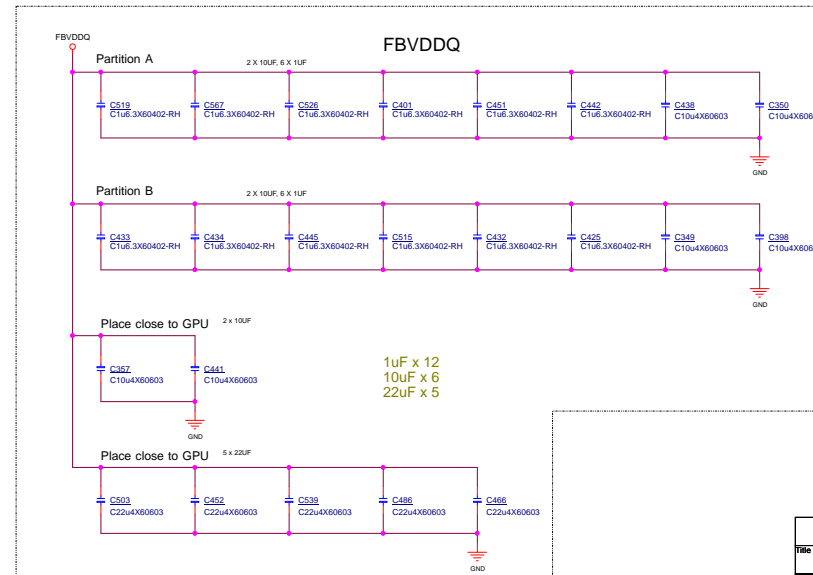
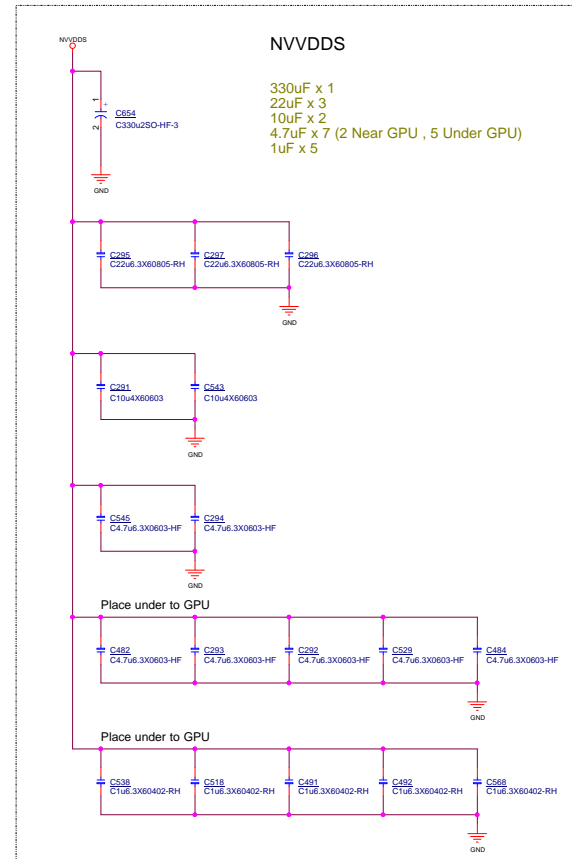
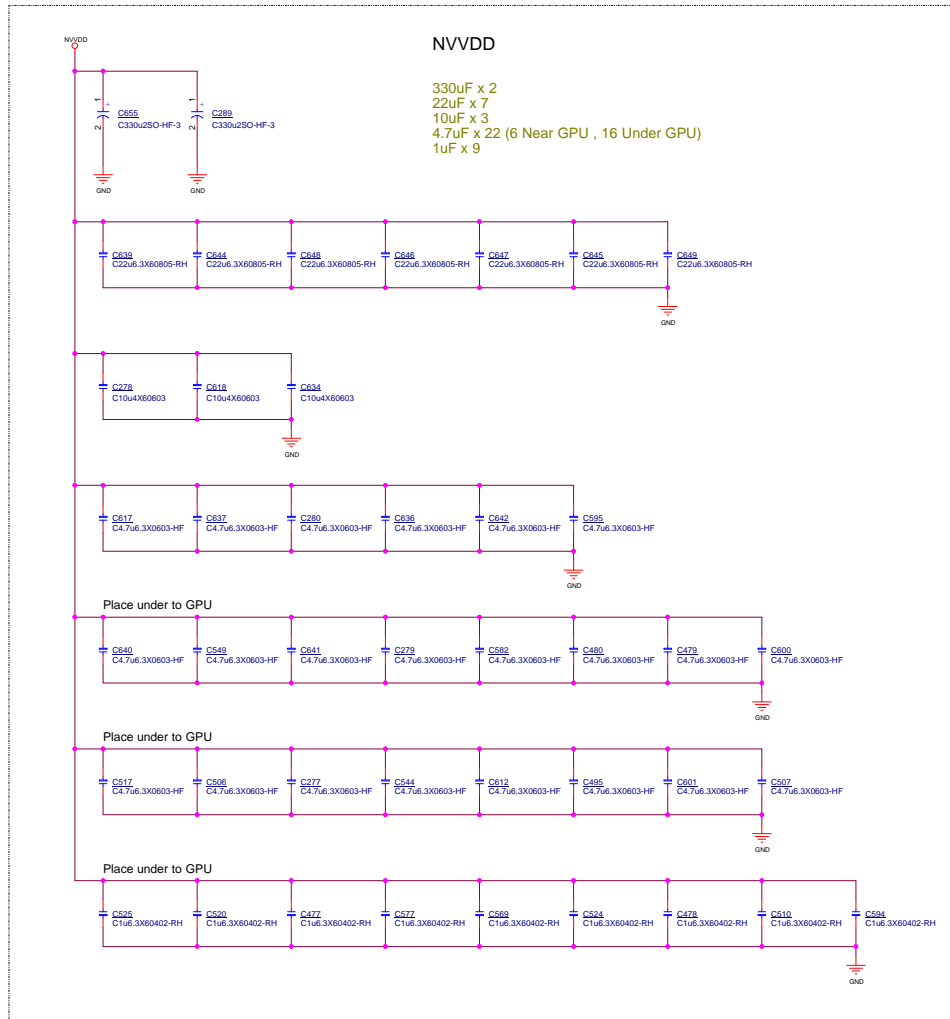


DGPU GND



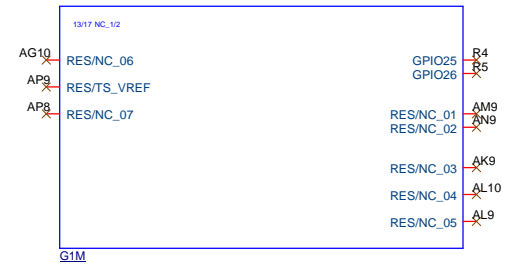
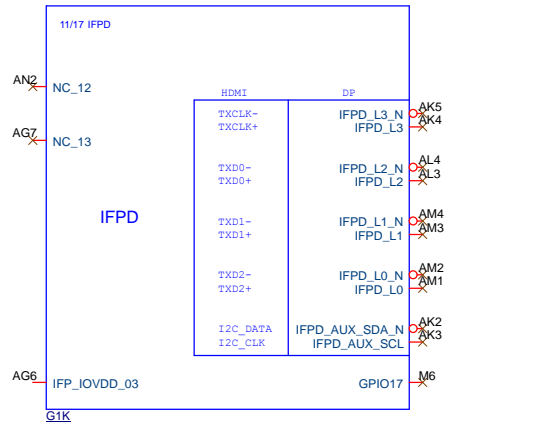
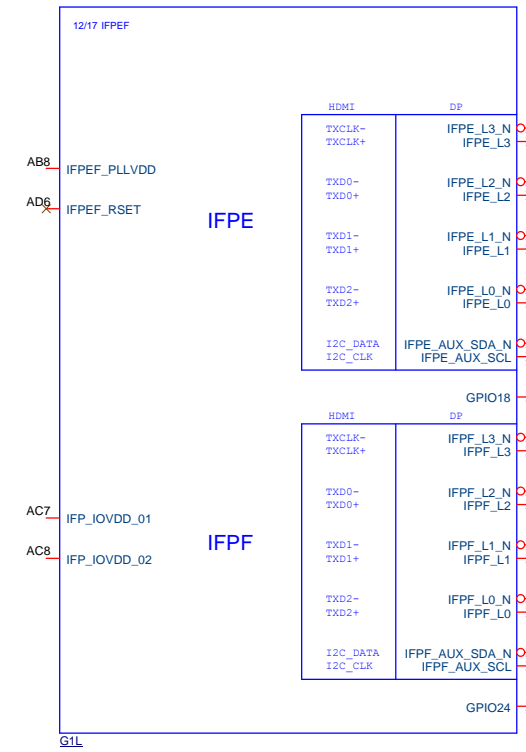
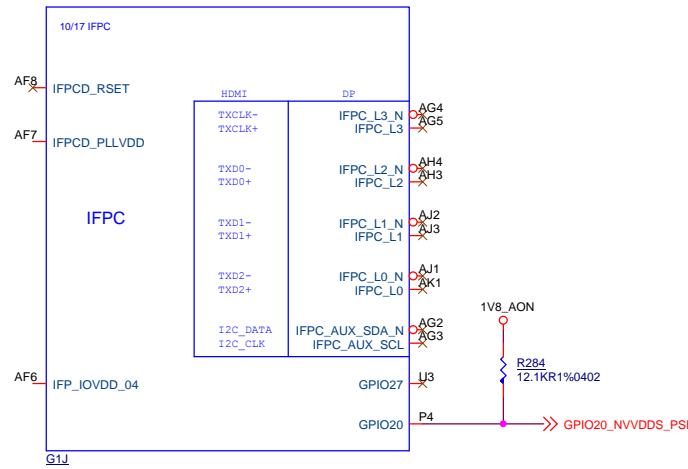
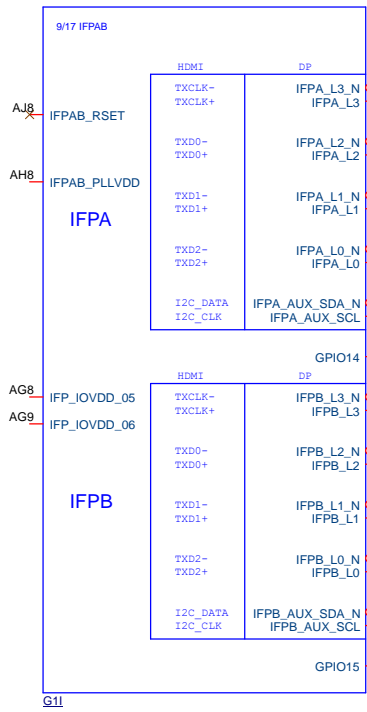


# GPU DECOUPLING



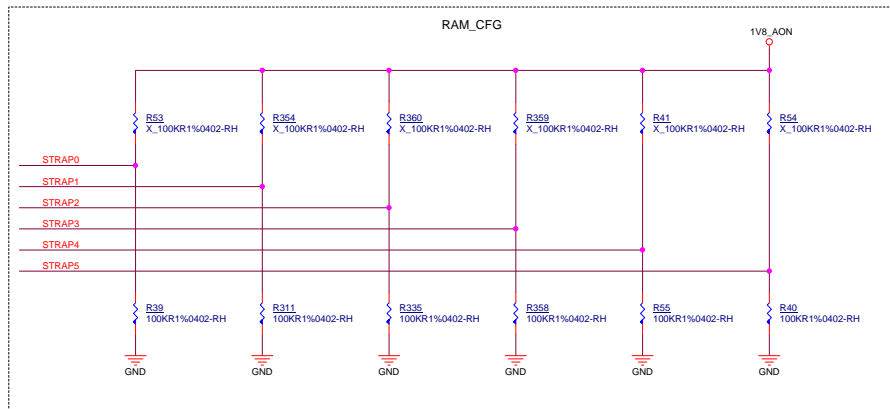
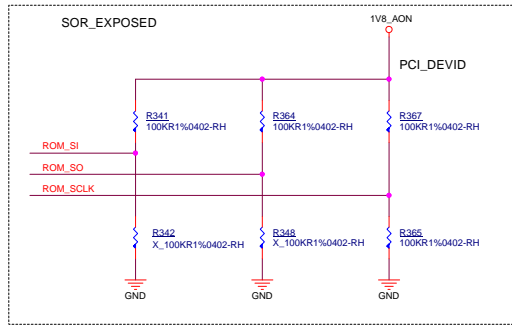
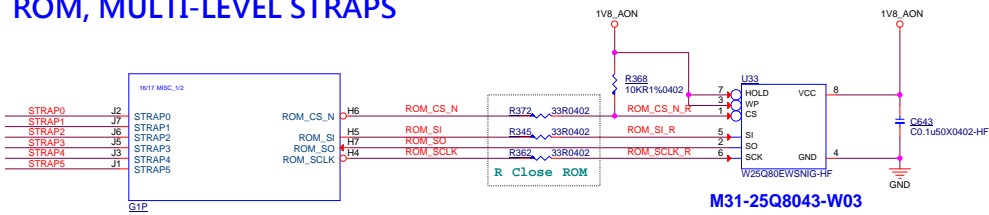


# DACA,Display IF





## ROM, MULTI-LEVEL STRAPS



STRAP0	STRAP1	STRAP2	RAMCFG[4:0]	STRAP Set
L	L	L	0x0 Samsung: M12-803254S-S02 / K4G80325FB-HC28	R39, R311, R335
H	L	L	0x1 Micron: MT51J256M32HF-70-A	R53, R311, R335
L	H	L	0x2 Hynix: M12-5GC8H05-H23 / H5GC8H24MJR-R0C	R39, R354, R335
H	H	L		
L	L	H		
H	L	H		
L	H	H	0x6 Hynix: M12-5GC4HG5-H23 / H5GC4H24AJR-R0C	R39, R354, R360
H	H	H	0x7 Samsung: M12-41325A5-S02 / K4G41325FE-HC28	R53, R354, R360
M	L	L	0x8 Micron: EDW4032BABG-70-F-A	R39, R53, R311, R335
L	M	L		

H=High :Tied to 1.8V  
M=Middle:Tied to 0.9V  
L=Low :Tied to 0V

ROM_SO	ROM_SI	ROM_SCLK	SOR_EXPOSED[3:0]	1:ENABLE 0:DISABLE
L	L	L	1111	DEFAULT SOR0/1/2/3 ENABLE
L	L	H	1110	
L	H	L	1101	
L	H	H	1100	
H	L	L	1011	
H	L	H	1010	
H	H	L	1001	
H	H	H	1000	
L	L	M	0111	
L	M	L	0110	
L	M	H	0101	
L	H	M	0100	
H	L	M	0011	
H	M	L	0010	
H	M	H	0001	
H	H	M	0000	V

STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
M	H	H	1	1	1	1
M	H	L	1	1	1	0
M	L	H	1	1	0	1
M	L	L	1	1	0	0
L	H	M	1	0	1	1
L	M	H	1	0	1	0
L	M	L	1	0	0	1
L	L	M	1	0	0	0
H	H	H	0	1	1	1
H	H	L	0	1	1	0
H	L	H	0	1	0	1
H	L	L	0	1	0	0
L	H	H	0	0	1	1
L	H	L	0	0	1	0
L	L	H	0	0	0	1 DEFAULT
L	L	L	0	0	0	0 v

```

1:SMB_ALT_ADDR ENABLE
0:SMB_ALT_ADDR DISABLE

1:DEVID_SEL REBRAND
0:DEVID_SEL ORIGINAL

1:PCIE_CFG LOW POWER
0:PCIE_CFG HIGH POWER

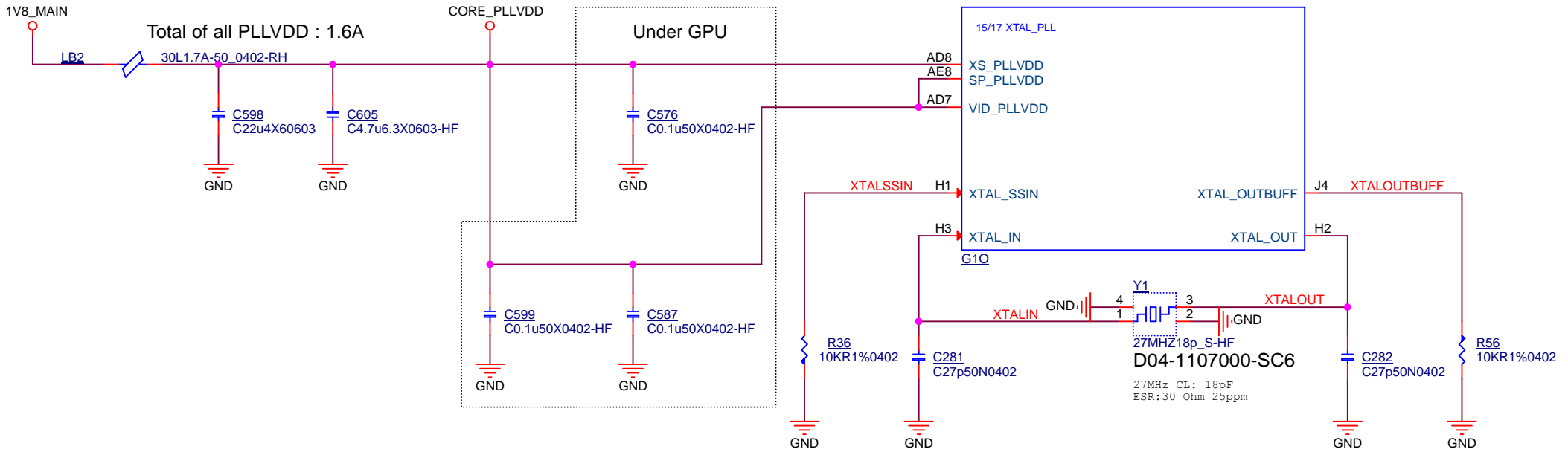
1:VGA_DEVICE ENABLE
0:VGA_DEVICE DISABLE

H=High :Tied to 1.8V
M=Middle:Tied to 0.9V
L=Low :Tied to 0V

```

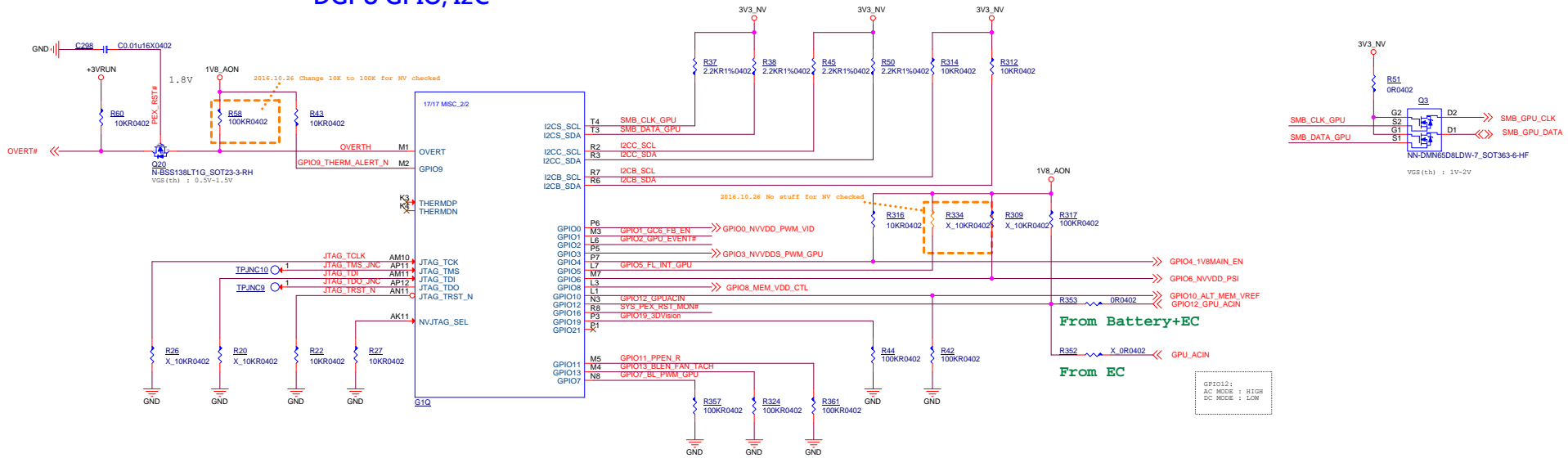


# DGPU XTAL

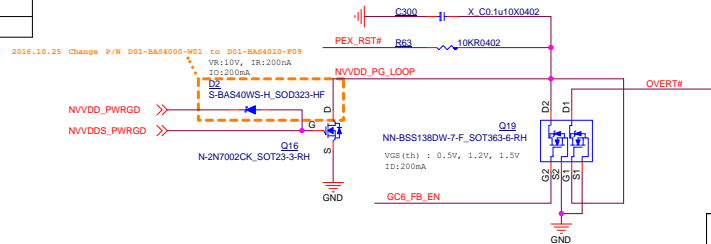
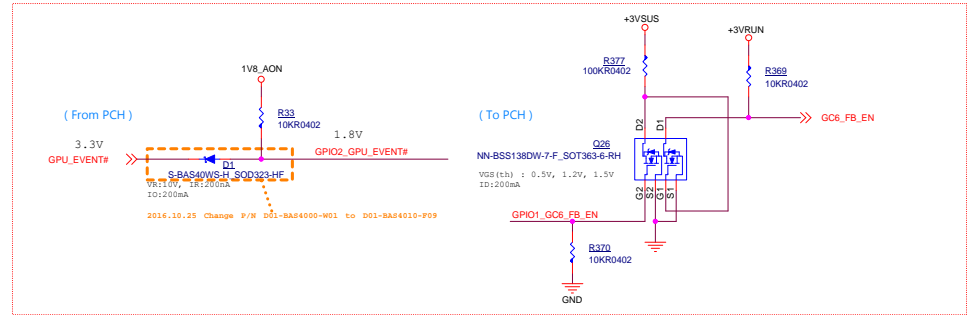
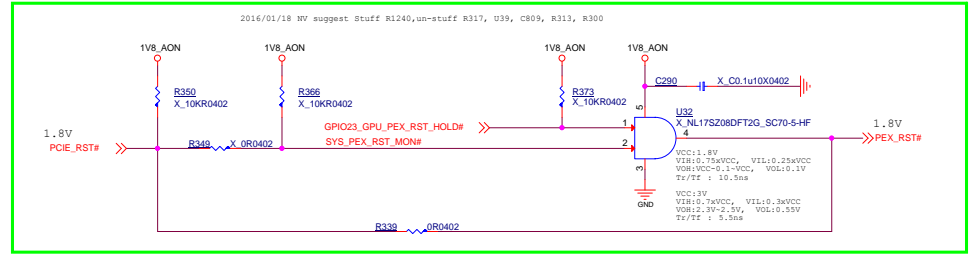




# DGPU GPIO, I2C



Pin Name	Normal function	I/O	Functional Description	Recommended Default Pull-up or Pull-down
GPIO0	PWR_VID	O	GPU Core VDD PWM control signal	0 to 1V8 PWM output
GPIO1	GC6_FB_EN	O	FB Enable for GC6 2.1	OD, 10K pull-down
GPIO2	GPU_EVENT#	I	GPU wake signal for GC6 2.1	10K pull-up to 1V8_AON
GPIO3	NVVD_SRAM_PWM	O	PWM output to control the SRAM power supply	0 to 1V8 output
GPIO4	1V8_MAIN_EN	O	GPU POWER Sequencing for GC6 2.1	OD, 10K pull-up to 1V8_AON
GPIO5	FRM_LCK#	I	Active low Frame Lock	OD, 1V8 pull-up to 1V8_AON
GPIO6	NVVD_PSI	O	Phase shedding	10K pull-up to 1V8_AON
GPIO7	LCD_BL_PWM	O	Panel Backlight PWM Brightness Control	100K pull-down
GPIO8	MEM_VDD_CTL	O	Memory Voltage Control	pull-up/pull-down to set the FWDD/O power-on voltage
GPIO9	THERM_ALERT	I/O	Active Low Thermal Alert	OD, 10K pull-up to 1V8_AON
GPIO10	MEM_VREF_CTL	O	Memory VREF Control	100K pull-down
GPIO11	LCD_VCC	O	Panel Power Enable	100K pull-down
GPIO12	PWR_LEVEL	I	AC power detect or power supply overdraw input	100K pull-up to 1V8_AON
GPIO13	LCD_BLEN	O	Panel Backlight Enable	100K pull-down
GPIO14	HPD_A	I	Hot Plug Detect for IFPA	
GPIO15	HPD_B	I	Hot Plug Detect for IFPB	
GPIO16	SYS_PEX_RST_MON#	O	System side PCIe reset monitor	10K pull-up to 1V8_AON
GPIO17	HPD_D	I	Hot Plug Detect for IFPD	
GPIO18	HPD_E	I	Hot Plug Detect for IFPE	
GPIO19	3Dvision	O	3D Vision L/R signal	100K pull-down
GPIO20	GC5_MODE	I/O		
GPIO21	UNUSED	I/O		
GPIO22	UNUSED	I/O		
GPIO23	GPU_PEX_RST_HOLD#	O	GPU PCIe self-reset control	OD, 10K pull-up to a gated 3V3
GPIO24	HPD_F	I		
GPIO25	UNUSED			
GPIO26	UNUSED			
GPIO27	HPD_C	I	Hot Plug Detect for IFPC	

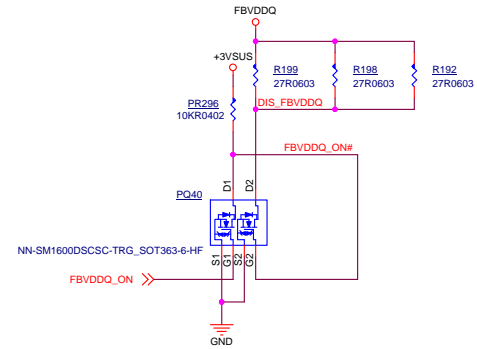
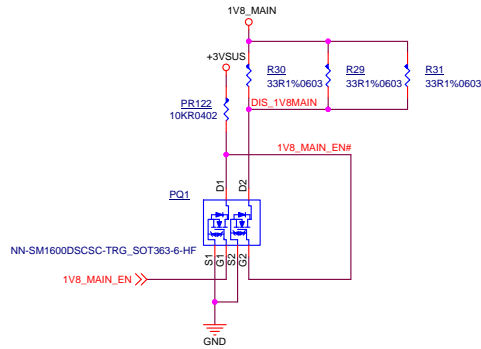
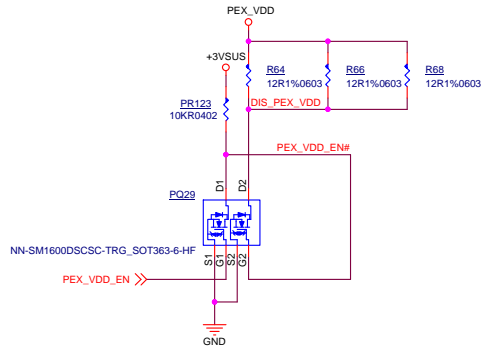
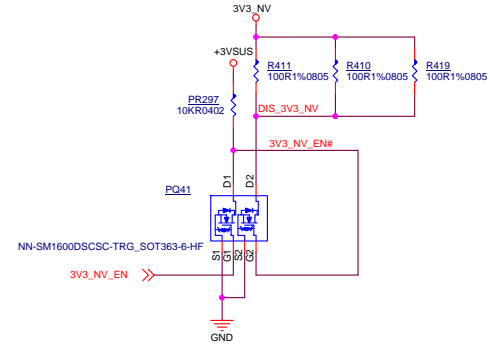
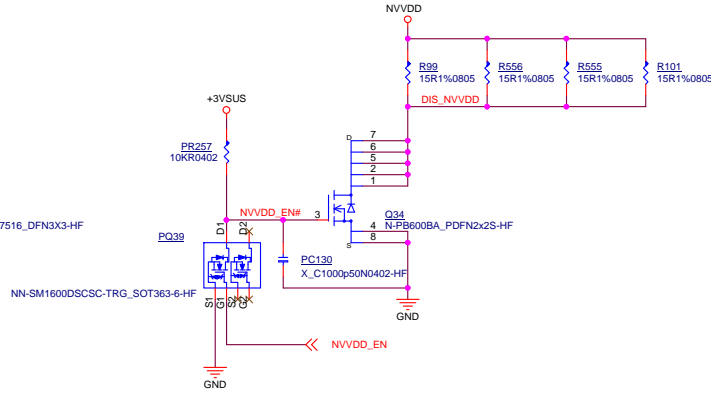
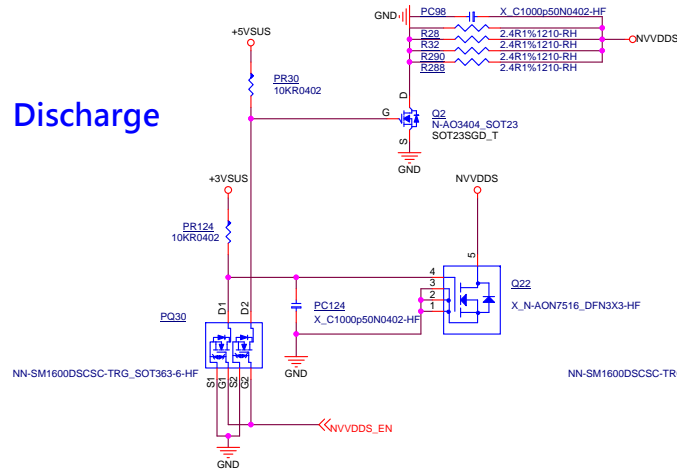




**Power Off=NVVDDS/PEX\_VDD/FBVDDQ(鎖順序) -> NVVDD/ NV可同時掉 )-> 1V8\_MAI N-> 1V8\_AON**



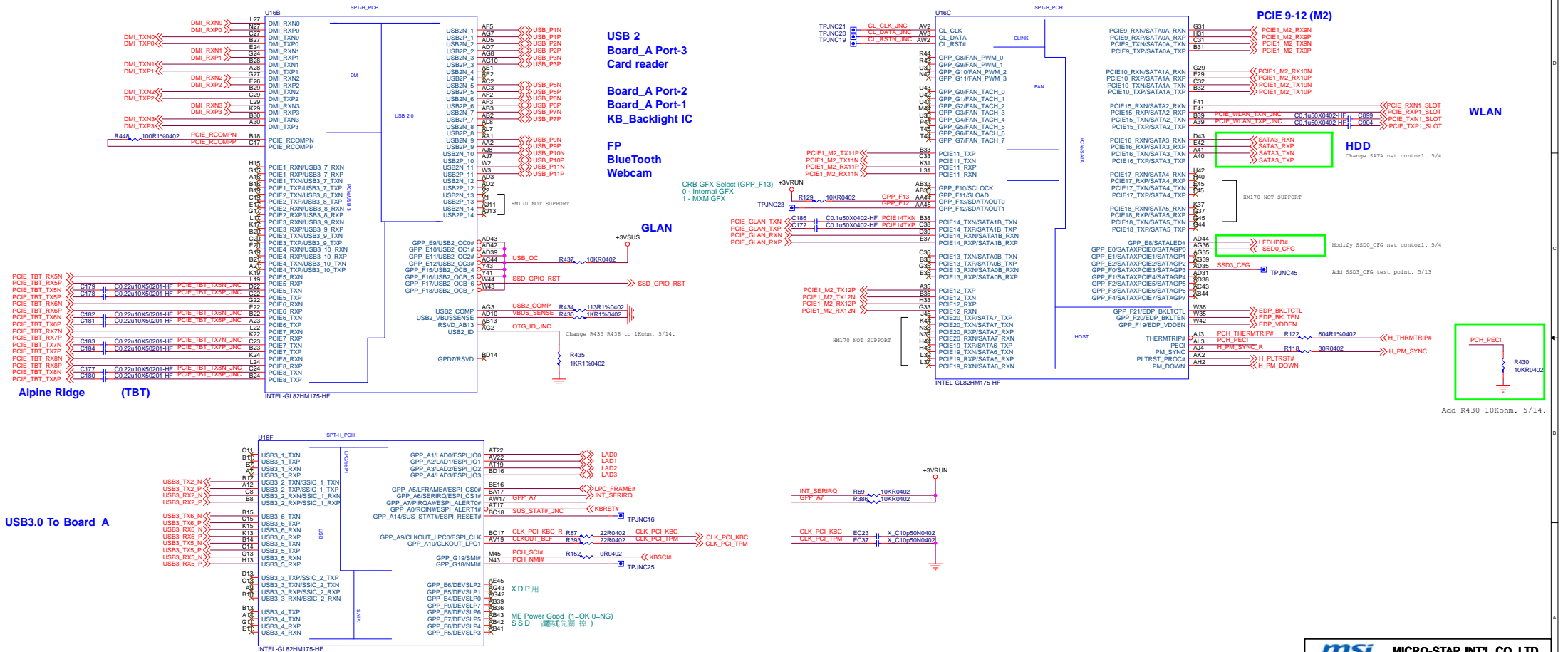
# Discharge



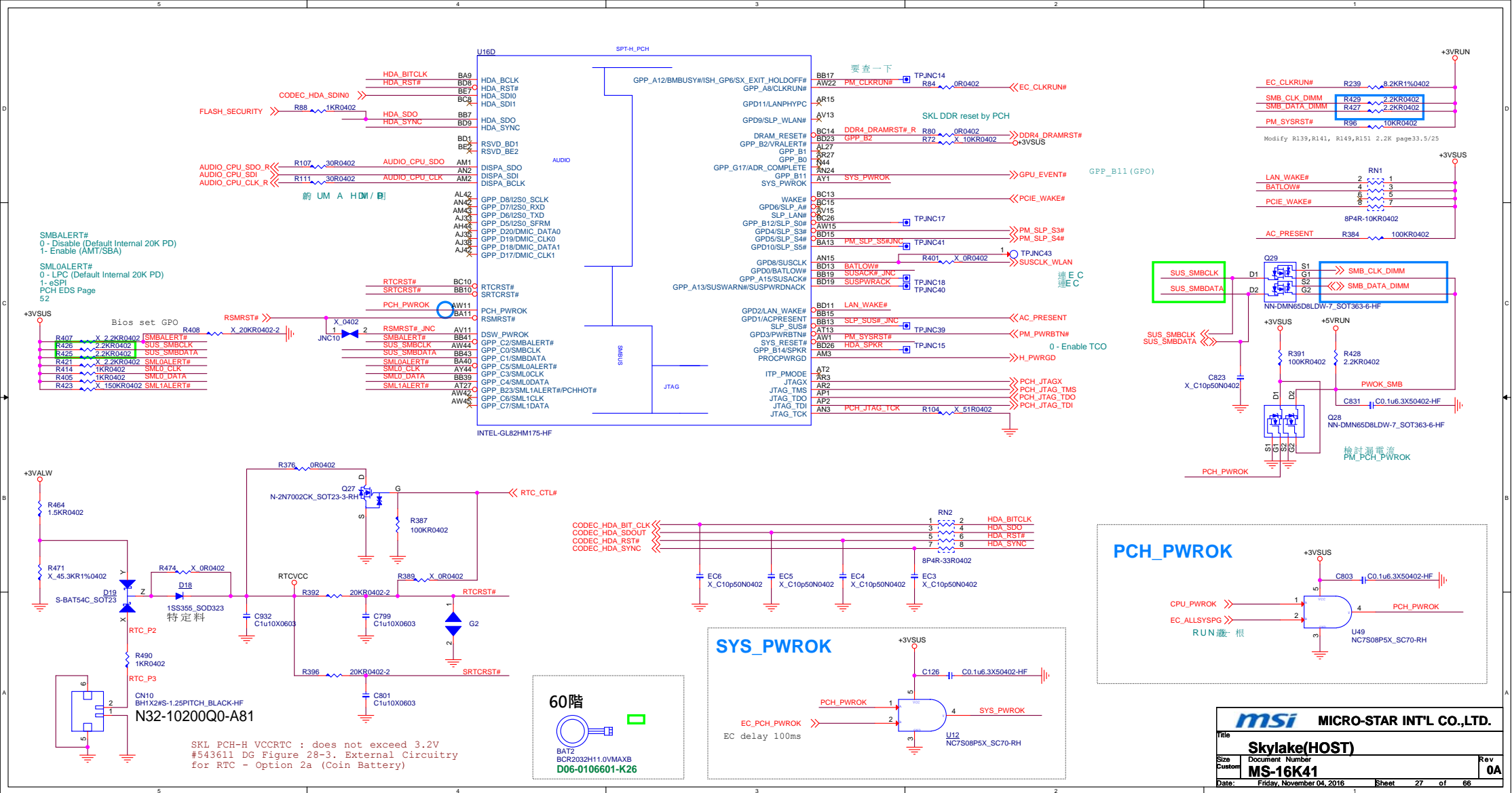




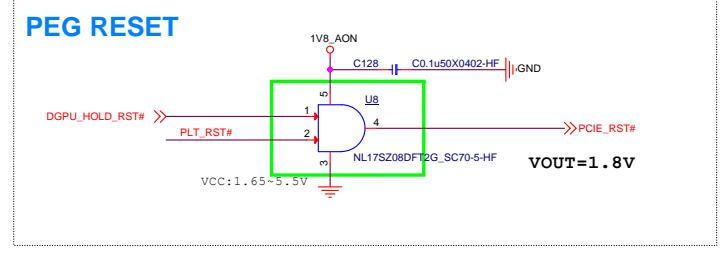
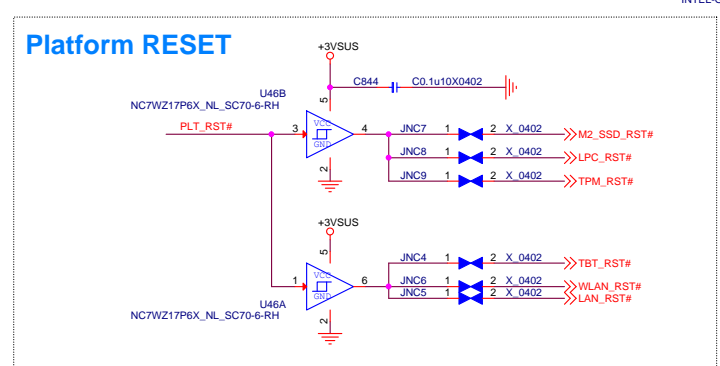
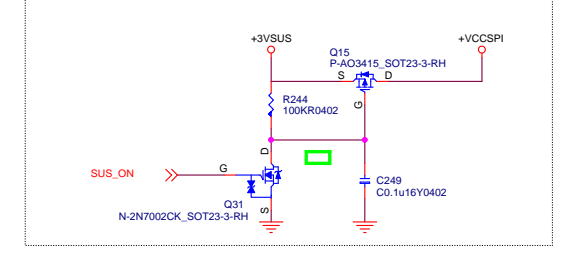
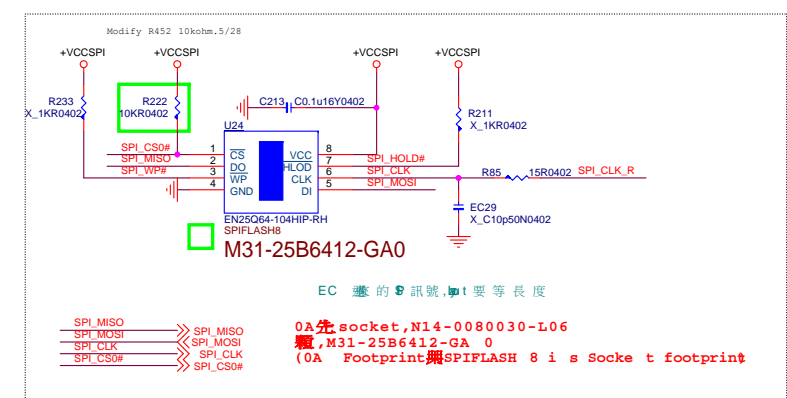
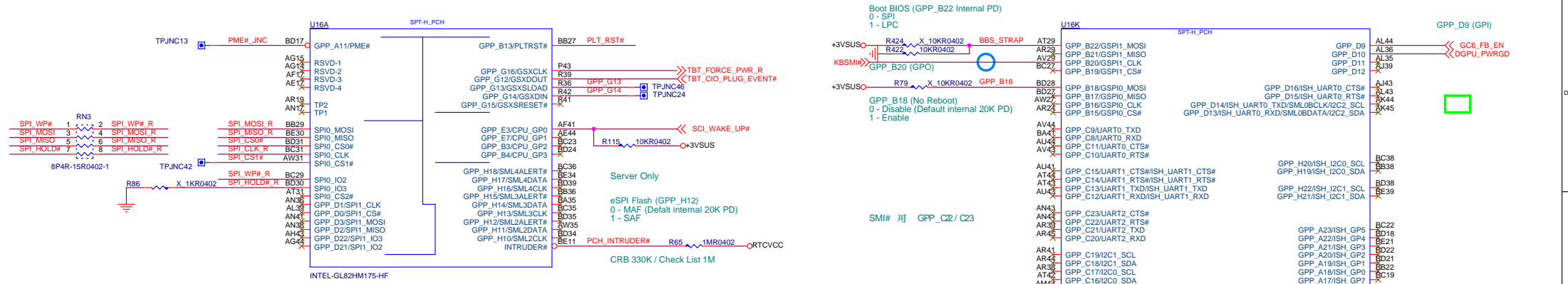






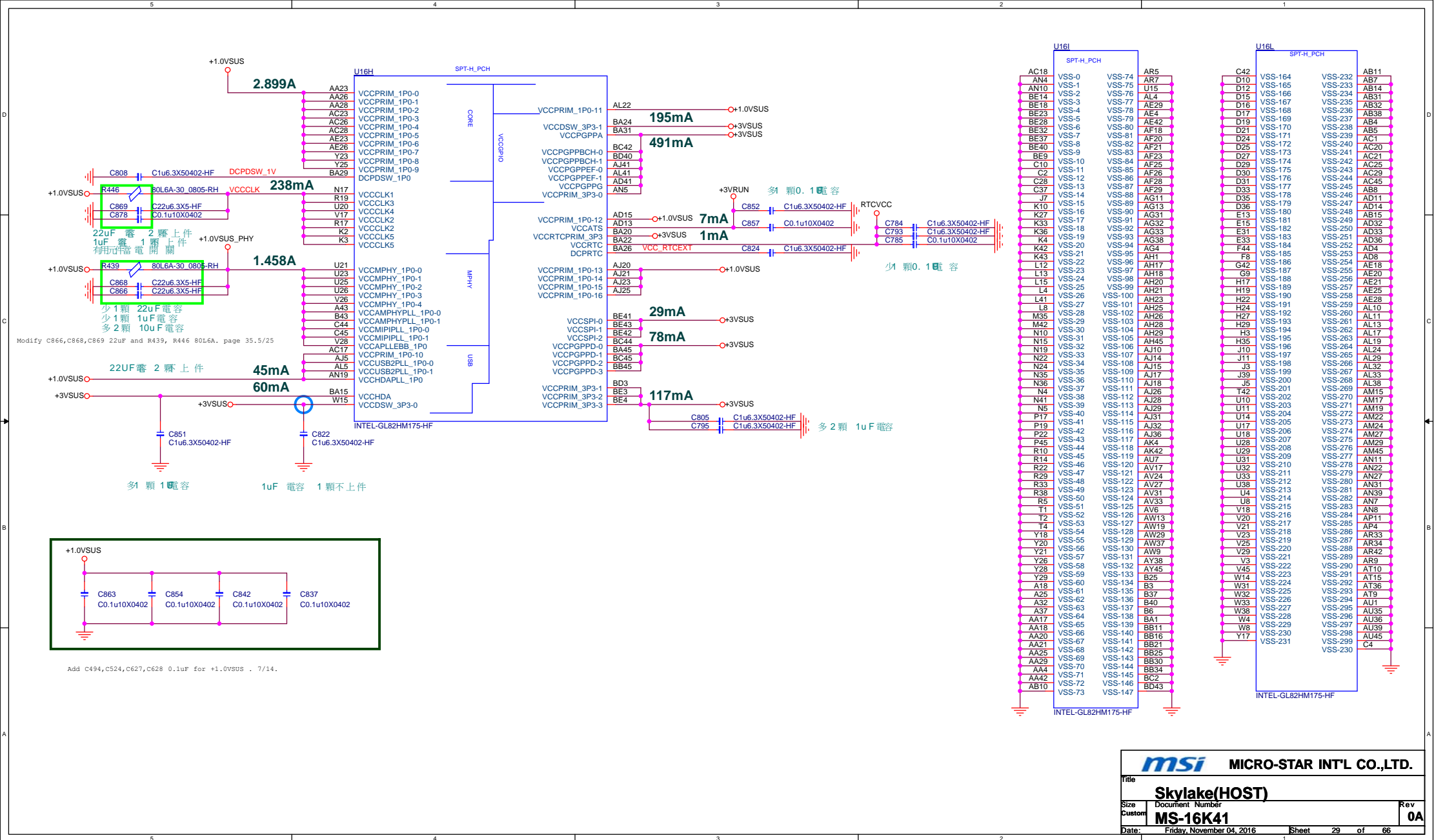






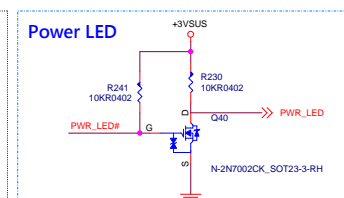
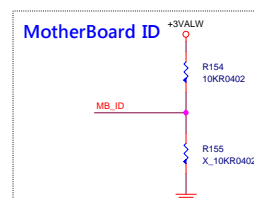
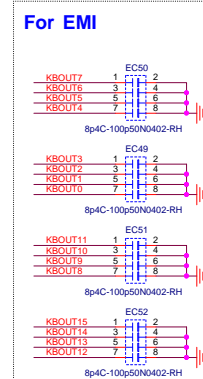
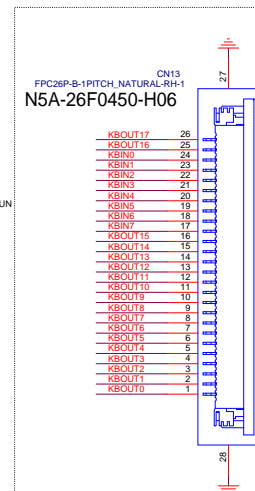
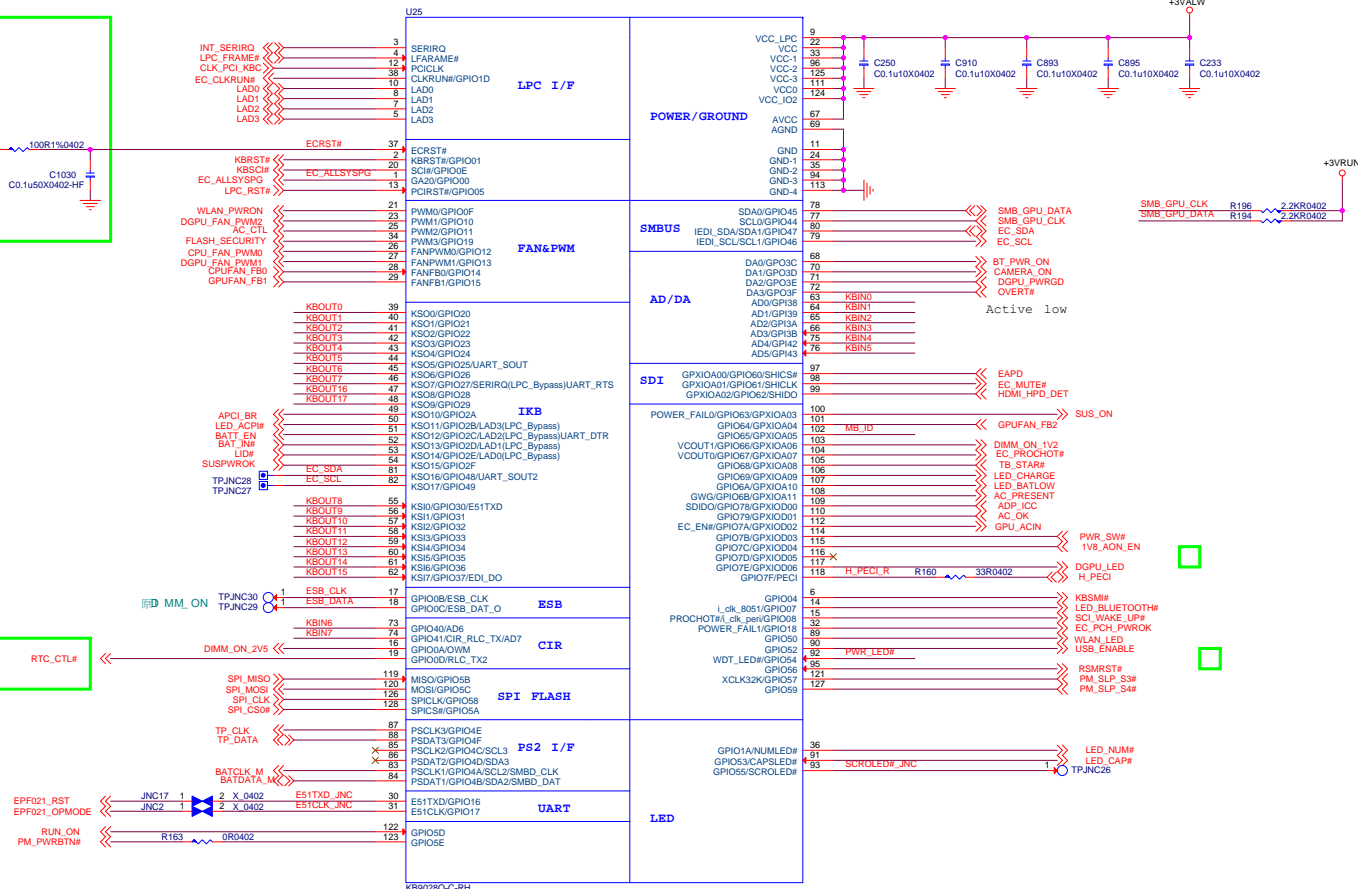
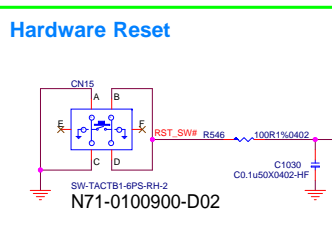
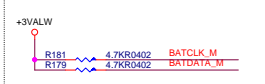
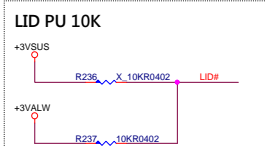
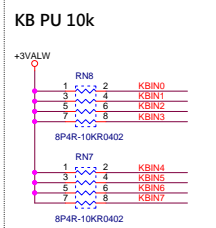
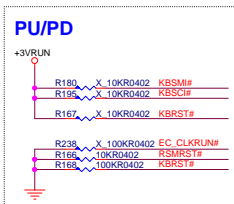
msi MICRO-STAR INT'L CO.,LTD.			
Title	Skylake(HOST)		
Size	Document Number	Rev	
Custom	MS-16K41	0A	
Date:	Friday, November 04, 2016	Sheet	28 of 66







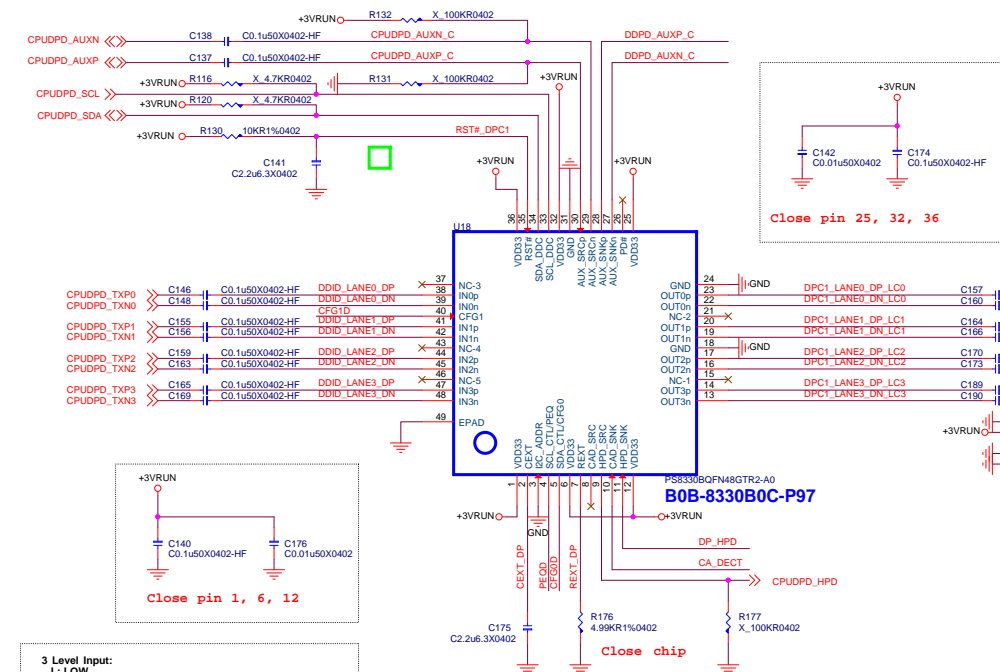
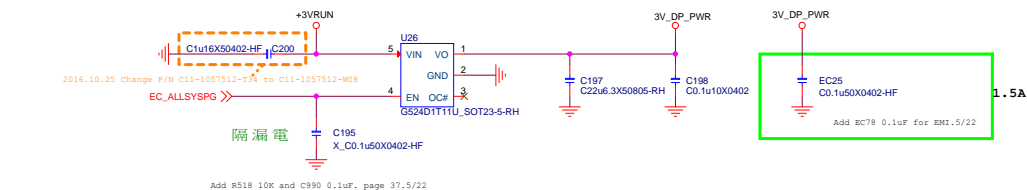
## KBC/EC/uP (ENE9028)





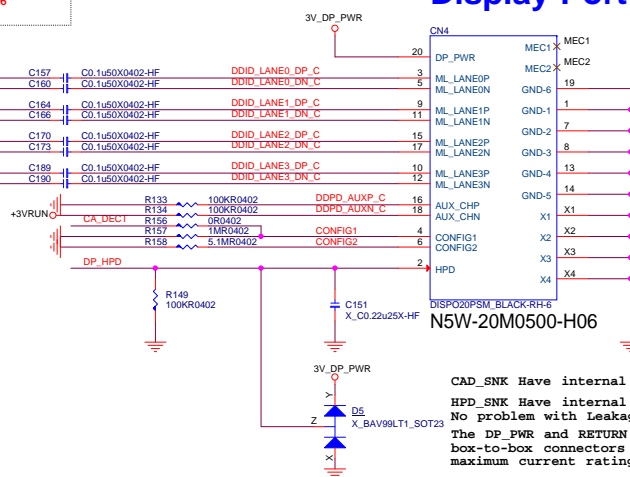
## Display Port

The preset trip limit must not exceed 3A at the Upstream device connector DP\_PWR pin and 1.5A at the Downstream device connector DP\_PWR pin.



Close pin 25, 32, 36

## Display Port



CAD\_SNK Have internal Pull down 1Mohm.  
HPD\_SNK Have internal Pull down 150kohm.  
No problem with Leakage from DP device  
The DP\_PWR and RETURN pins of the  
box-to-box connectors must support the  
maximum current rating of 500mA.

3 Level Input:  
L: LOW  
H: HIGH  
M: VDD33/2, connect both pull-up and pull-down resistors

Configuration pin for automatic EQ and AUX interception; Internal pull down at ~150k Ohm, 3.3V I/O.  
 L: default, automatic EQ enable & AUX interception enable  
 H: automatic EQ disable & AUX interception enable  
 M: automatic EQ disable & AUX interception disable, no pre-emphasis, 600mVpp swing

Configuration pin for auto test and input offset cancellation, 3.3V IO, internal pull up at ~150K Ohm

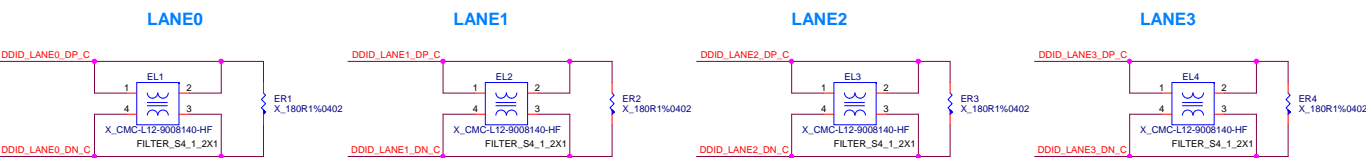
- H: default, auto test disable & input offset cancellation enable
- L: auto test enable & input offset cancellation enable
- M: auto test disable & input offset cancellation disable

```

Programmable input equalization levels; Internal pull down at ~150k Ohm, 3.3V I/O.
L: default, LEQ, compensate channel loss up to 12dB @ HBR2
H: HEQ, compensate channel loss up to 15dB @ HBR2
M: LLEQ, compensate channel loss up to 5dB @ HBR2

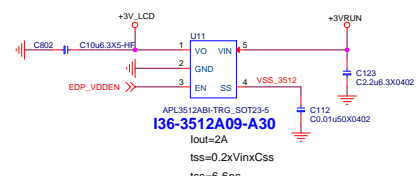
```

## EMI Close Connector

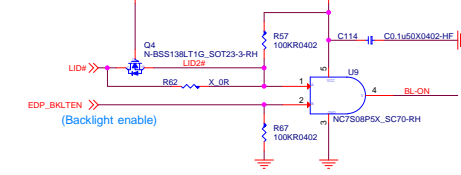




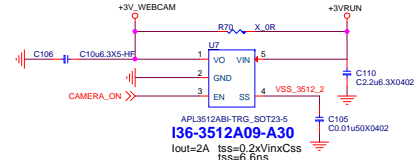
## Pannel Device Logic Power



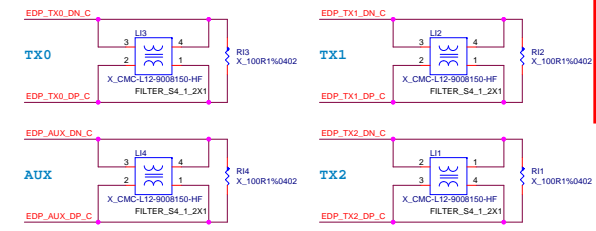
## Backlight



## CAMERA Power



## EMI Close Connector



**Note:** CMC-L12-9008150-HF/0/N : L12-9008150-F130 %  
Default Orcad library and footprint F130B\_S4\_1\_25X1  
are not match datasheet.

1 2 3 4

1 2 3 4

1 2 3 4

1 2 3 4

1 2 3 4

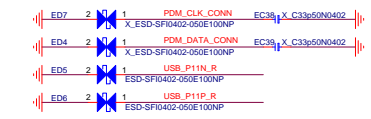
1 2 3 4

1 2 3 4

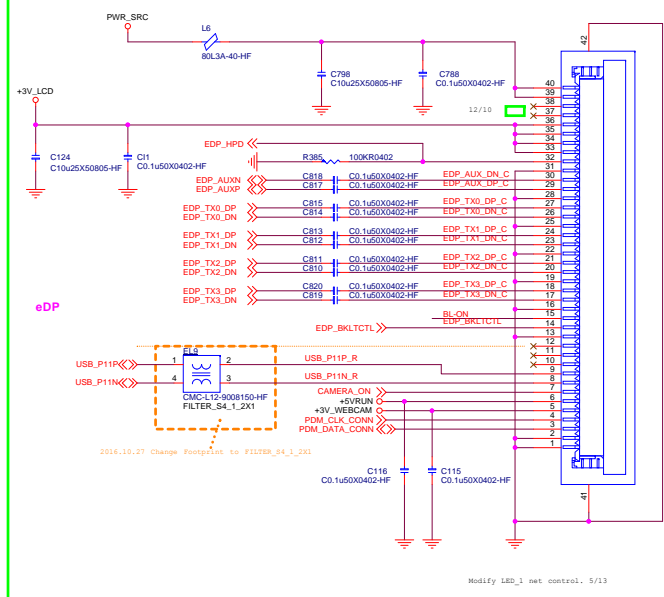
1 2 3 4

1 2 3 4

## ESD



## eDP Connector



CN12  
FP46P-0.5PITCH\_NATURAL-HF  
N5A-40F0180-A81

## LCD Module Pin Define FOR FULL HD PANEL

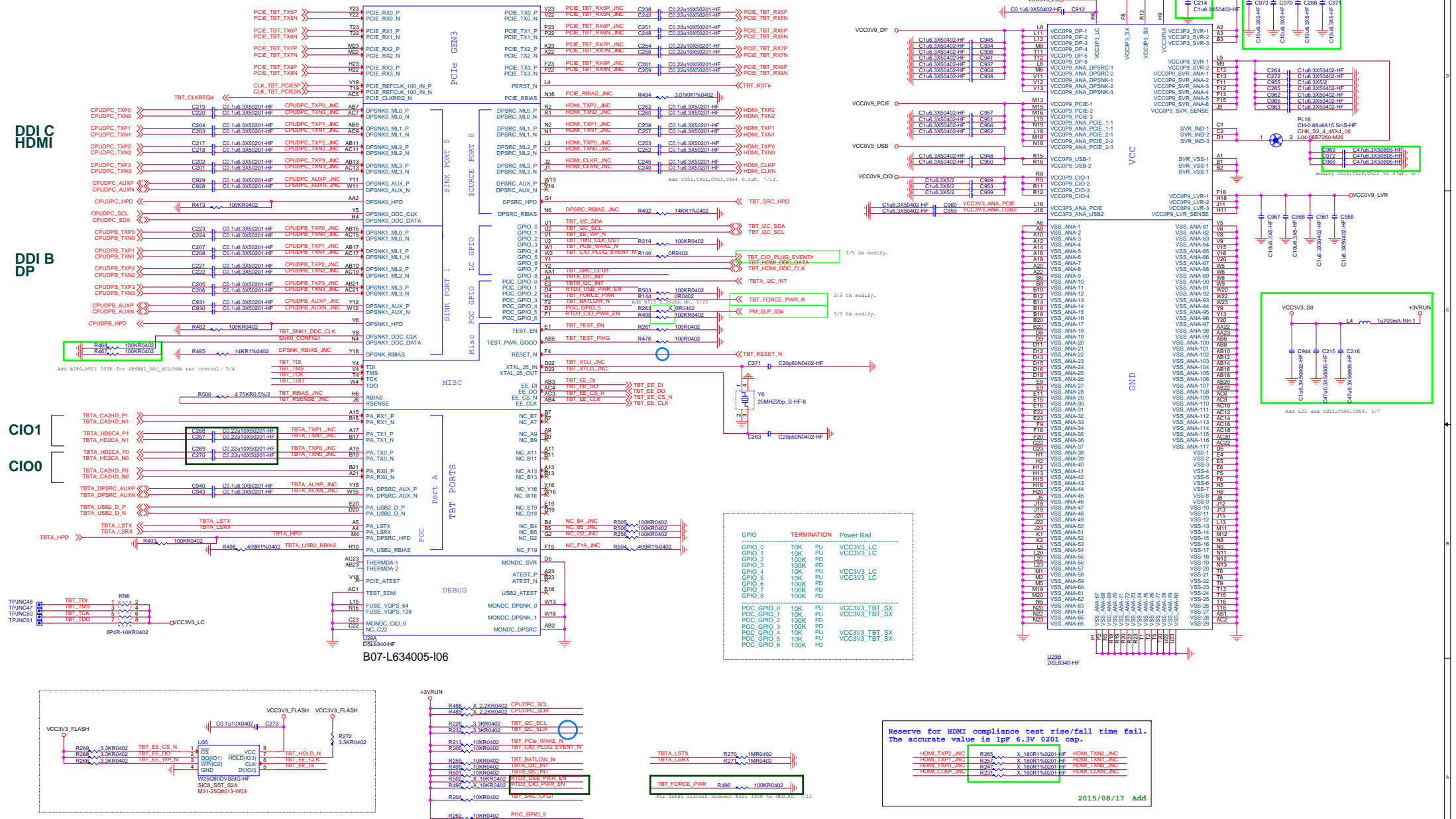
Pin No	Symbol	Description
1	Vcom SDA	Vcom IIC SDA
2	H_GND	High Speed Ground
3	LAN1_N	Complement Signal-Lane 1
4	LAN1_P	True Signal-Main Lane 1
5	H_GND	High Speed Ground
6	LAN0_N	Complement Signal-Lane 0
7	LAN0_P	True Signal-Main Lane 0
8	H_GND	High Speed Ground
9	AUX+	True Signal-Auxiliary Channel
10	AUX-	Complement Signal-Auxiliary Channel
11	H_GND	High Speed Ground
12	LCD_VCC	Power Supply +3.3 V (typical)
13	LCD_VCC	Power Supply +3.3 V (typical)
14	NC	No Connection (Reserved for CMI test)
15	H_GND	Ground
16	H_GND	Ground
17	HPD	Hot Plug Detect
18	BL_GND	BL Ground
19	BL_GND	BL Ground
20	BL_GND	BL Ground
21	BL_GND	BL Ground
22	BL_EN	BL_Enable Signal of LED Converter
23	BL_PWM	PWM Dimming Control Signal of LED Converter
24	Vcom SCL	Vcom IIC SCL
25	NC	No Connection (Reserved)
26	LED_VCCS	BL Power
27	LED_VCCS	BL Power
28	LED_VCCS	BL Power
29	LED_VCCS	BL Power
30	NC	No Connection (Reserved)

## LCD Module Pin Define FOR WQHD PANEL

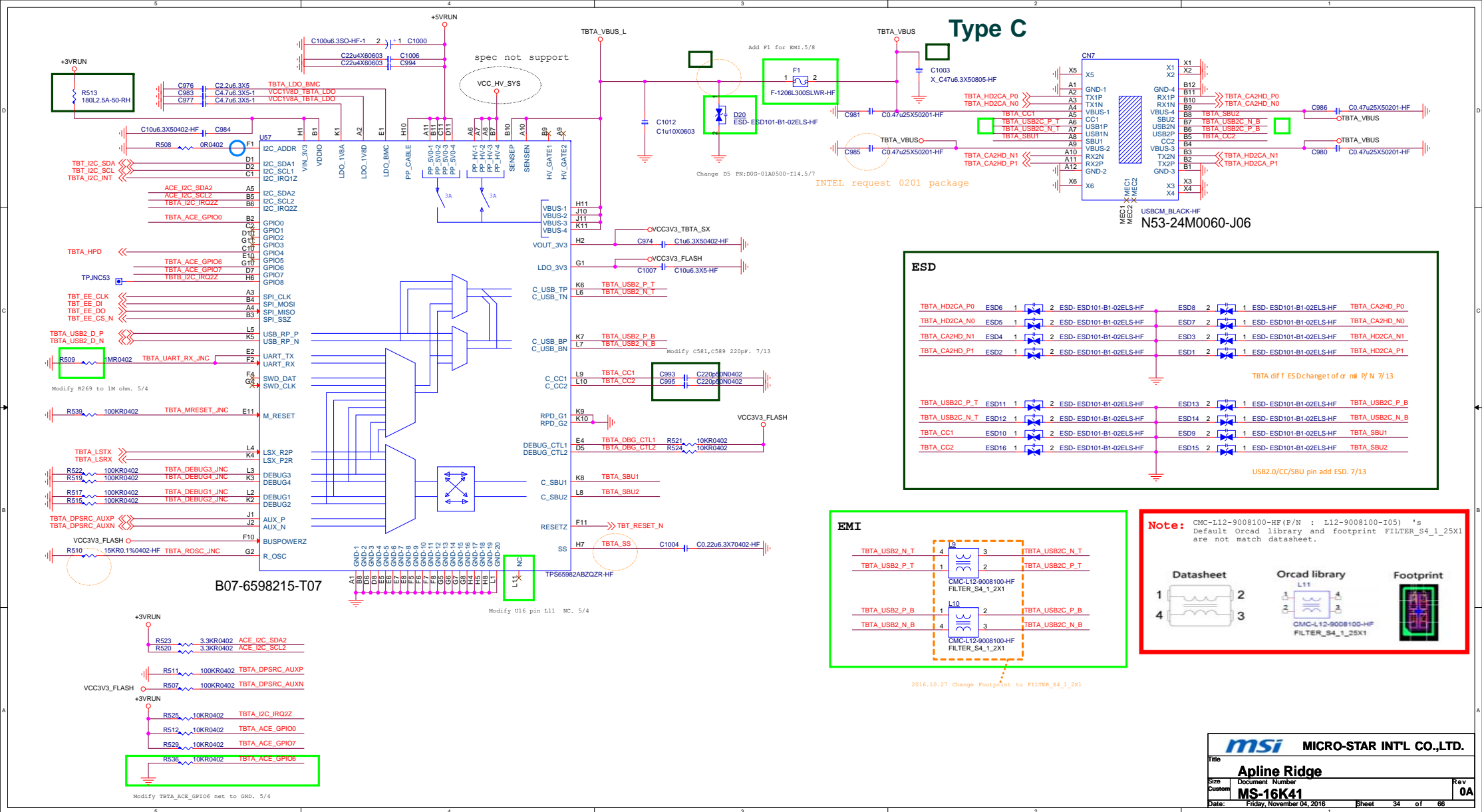
Pin No	Symbol	Description
1	NC	Reserved for LCD manufacturer's use
2	H_GND	High Speed Ground
3	Lane3_N	Complement Signal Link Lane 3
4	Lane3_P	True Signal Link Lane 3
5	H_GND	High Speed Ground
6	Lane2_N	Complement Signal Link Lane 2
7	Lane2_P	True Signal Link Lane 2
8	H_GND	High Speed Ground
9	Lane1_N	Complement Signal Link Lane 1
10	Lane1_P	True Signal Link Lane 1
11	H_GND	High Speed Ground
12	LCD_VCC	Complement Signal Link Lane 0
13	Lane0_P	True Signal Link Lane 0
14	H_GND	High Speed Ground
15	AUX_CH_P	True Signal Auxiliary Channel
16	AUX_CH_N	Complement Signal Auxiliary Channel
17	H_GND	High Speed Ground
18	VDD	
19	VDD	
20	VDD	
21	VDD	
22	BIST	BIST patterns selection L : Disable [default] , H : Enable
23	LCD_GND	LCD logic and driver ground
24	LCD_GND	LCD logic and driver ground
25	LCD_GND	LCD logic and driver ground
26	LCD_GND	LCD logic and driver ground
27	HPD	HPD signal pin
28	BL_GND	Backlight ground
29	BL_GND	Backlight ground
30	BL_GND	Backlight ground
31	BL_GND	Backlight ground
32	BL_ENABLE	Backlight On/Off
33	BL_PWM_DIM	System PWM
34	NC	Reserved for LCD manufacturer's use
35	NC	Reserved for LCD manufacturer's use
36	VBL	Backlight power
37	VBL	Backlight power
38	VBL	Backlight power
39	VBL	Backlight power
40	NC	No Connection (Reserved)



## Thunderbolt

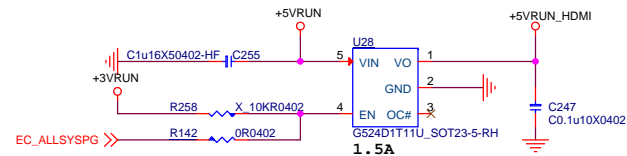








HDMI19PM\_BLACK-RH-10  
N5Y-19M0681-AF2



**TX0**

HDMI\_TXP0

1 2

4 3

X\_CM\_CMC-L12-9008140-HF  
FILTER\_S4\_1\_2X1

HDMI\_TXN0

ER6  
X\_180R1%0402

**TX1**

HDMI\_TXP1

1 2

4 3

X\_CM\_CMC-L12-9008140-HF  
FILTER\_S4\_1\_2X1

HDMI\_TXN1

ER7  
X\_180R1%0402

**TX2**

HDMI\_TXP2

1 2

4 3

X\_CM\_CMC-L12-9008140-HF  
FILTER\_S4\_1\_2X1

HDMI\_TXN2

ER8  
X\_180R1%0402

**CLK**

HDMI\_CLKP

1 2

4 3

X\_CM\_CMC-L12-9008140-HF  
FILTER\_S4\_1\_2X1

HDMI\_CLKN

ER5  
X\_180R1%0402



[illegible]

Schematic diagram of the LED driver circuit for the N5A-04F0330-A81 module. The circuit includes a transformer (CN11), a +5VSUS power source, and two LEDs (ED2 and ED1) connected to a hybrid LED driver (Q17). The driver is configured for H->L active mode. A truth table is provided for the H, L, and GREEN signals.

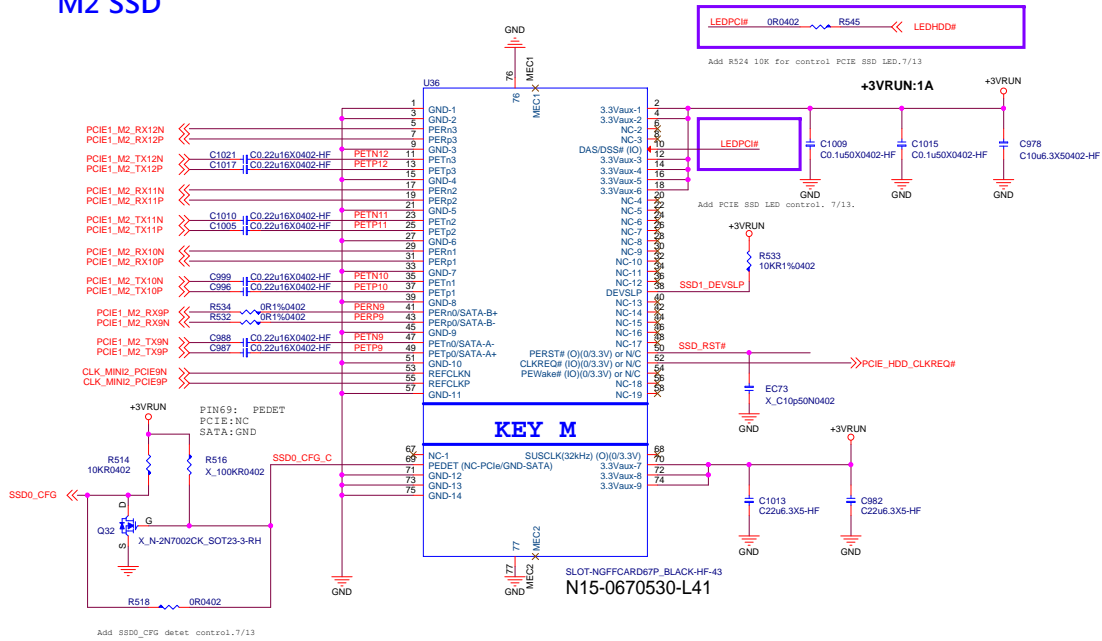
H	L	GREEN
L	L	X

Schematic diagram of the GPU\_FAN control circuit. The circuit includes a +3VRUN supply connected to a network of capacitors (C95, C118, C113) and a resistor (R52). The +5VRUN supply is connected to capacitors C118 and C113. The output of the +3VRUN network is labeled GPU\_FAN\_FB1. The output of the +5VRUN network is labeled DGPU\_FAN\_PWM1. Both signals are connected to a 6-pin connector CN1 (N32-1040AL0-A81) which is plugged into a fan. The fan is grounded to GND.

The diagram shows the electrical connection between the N5A-06F0310-A81 module and the 3/14 SWAR module. The module's pins are connected to a common ground and a +5VUS supply. A 30mA current source is connected to the module's pins. The circuit includes a 160R1% resistor (R415) and a 160R1% resistor (R416). The LED is connected to the 3/14 SWAR module. The module is labeled FPC2 X\_FPC6P-B-1PITCH\_WHITE-RH-2 N5A-06F0310-A81. The circuit also includes a 3/14 SWAR module and a 30mA current source.

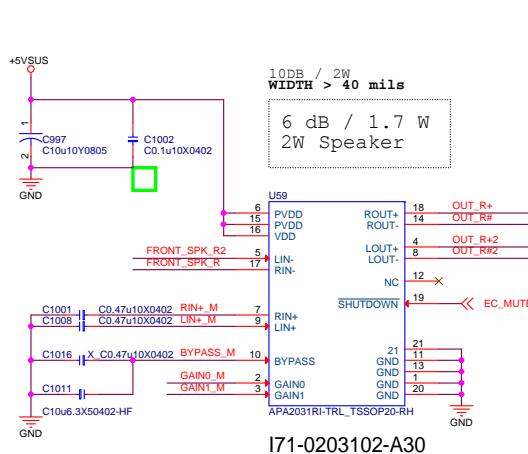
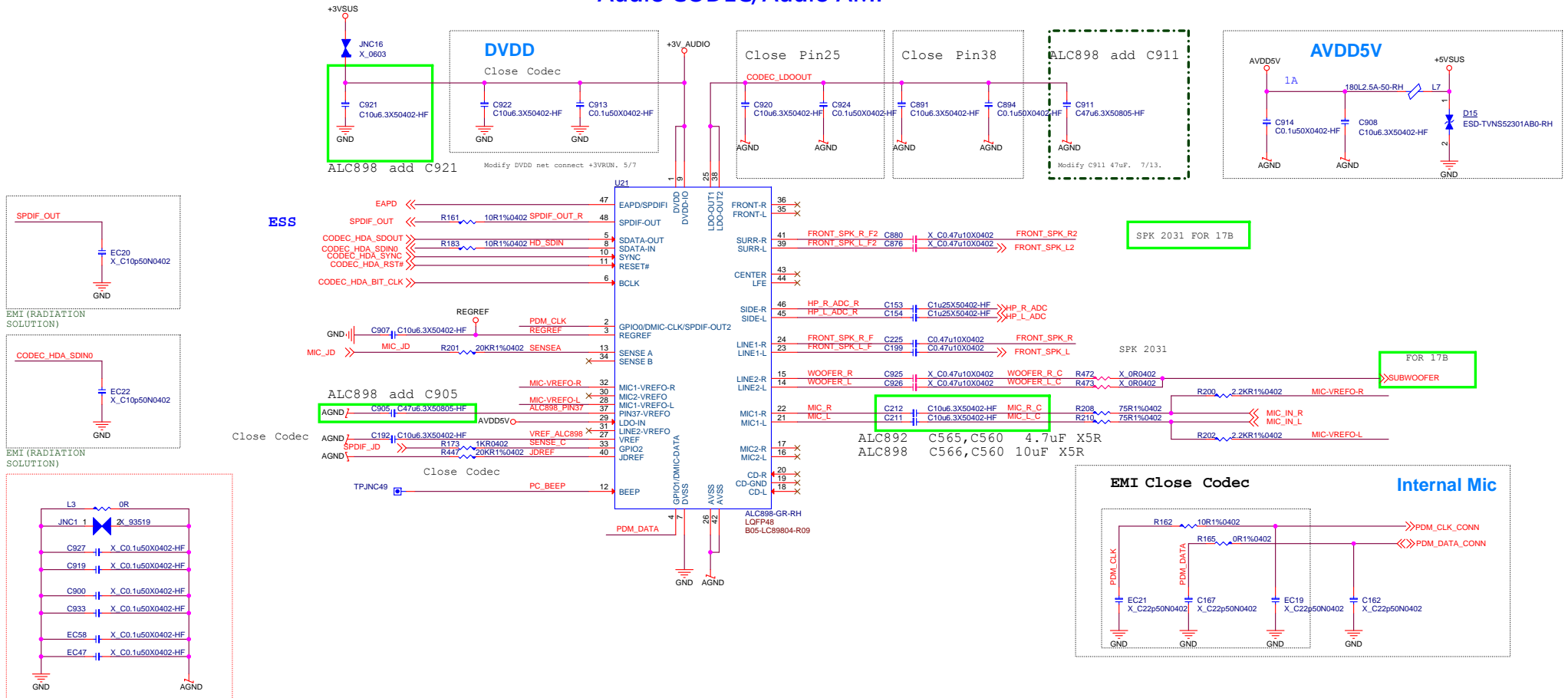


## M2 SSD





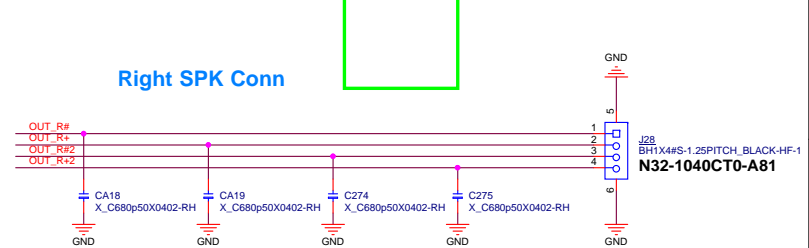
# Audio CODEC/Audio AMP



For APA2031

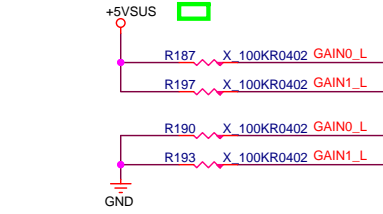
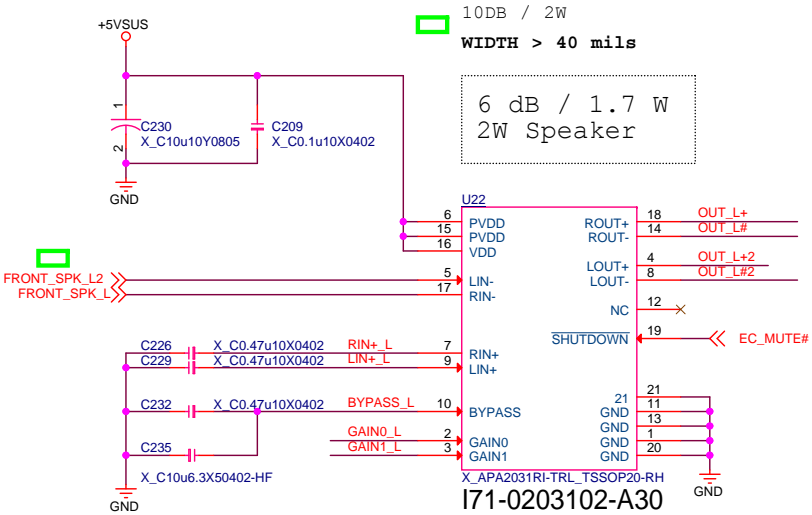
Av	GAIN0	GAIN1
6dB	0	0
10dB	0	1
15.6dB	1	0
21.6dB	1	1
4.3dB	X	X

Components: R526, R530, R527, R531.



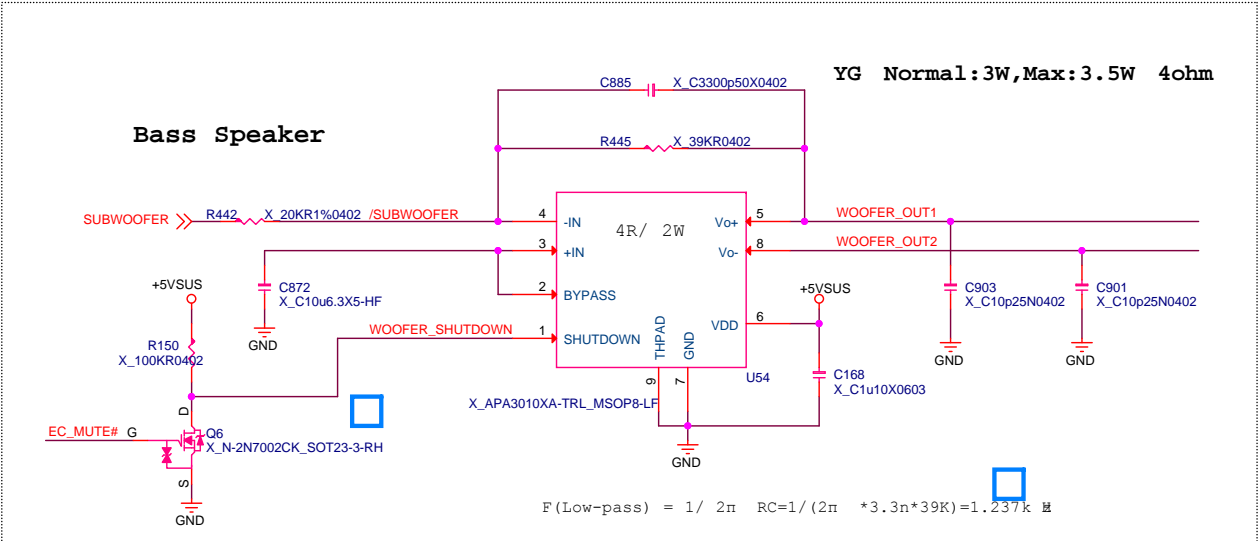
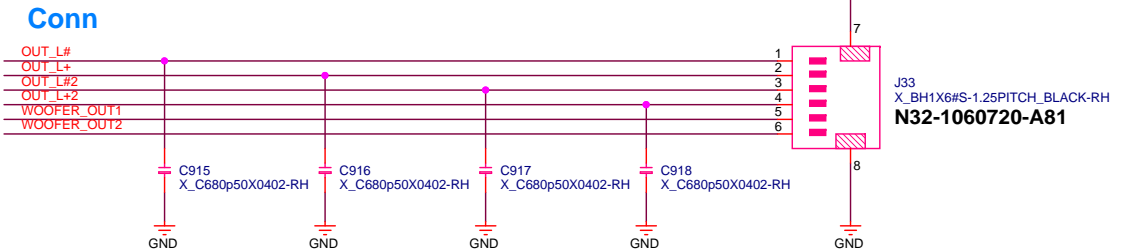


SPK LEFT /WoffeR FOR 17B



For APA2031

Av	GAIN0	GAIN1
6dB	0	0
10dB	0	1
15.6dB	1	0
21.6dB	1	1
4.3dB	X	X



MICRO-STAR INT'L CO.,LTD.

Title

SPK LEFT/WOOFER

Size

Document Number

MS-16K41

Rev

0A

Date:

Friday, November 04, 2016

Sheet

39

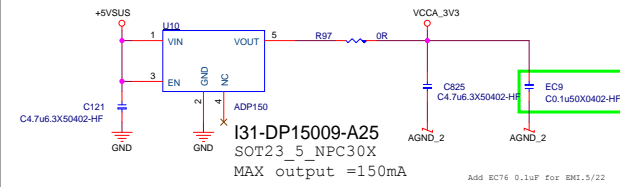
of

66

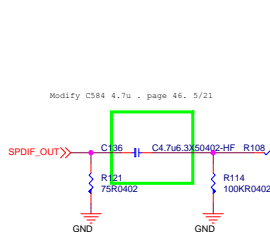


## ES9016K2M

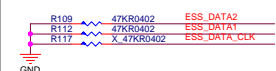
## ESS\_VCCA\_3V3



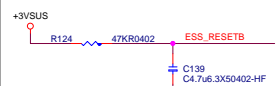
Change U18 to C74HC1GU04. 5/20



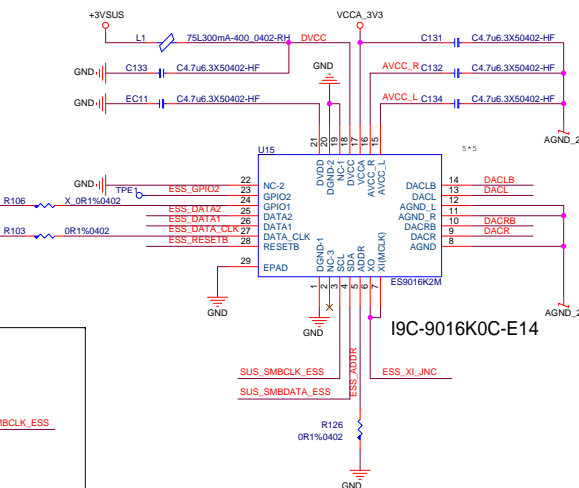
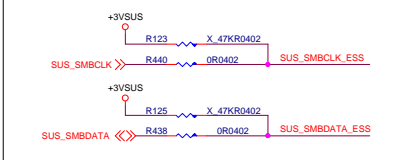
## DATA\_IN/OUT\_Select



## ESS\_RESET#

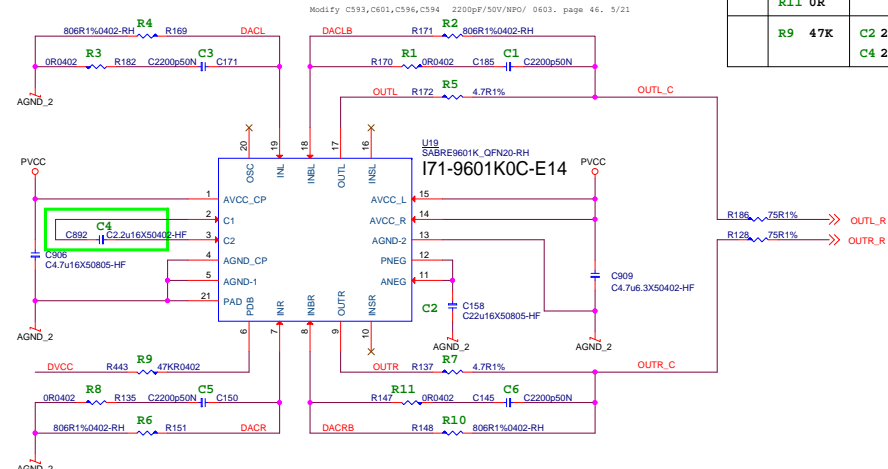
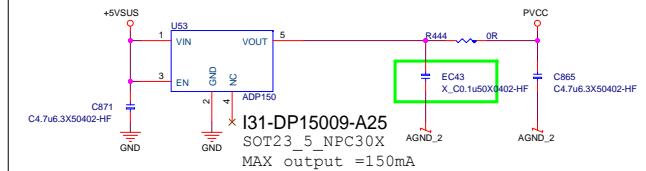


## ESS\_SMBUS



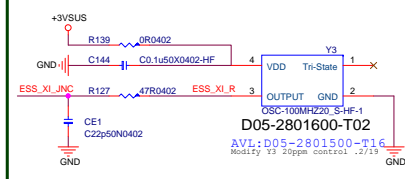
## SABRE9601K

## ESS\_PVCC



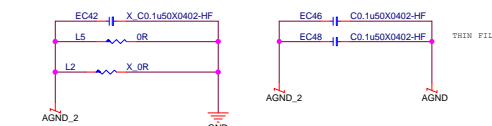
L-CH	R1	0R	C1	2200p
	R2	806R	C3	2200p
	R3	0R		
	R4	806R		
	R5	4.7R		
R-CH	R6	806R	C5	2200p
	R7	4.7R	C6	2200p
	R8	0R		
	R10	806R		
	R11	0R		
	R9	47K	C2	22u
			C4	2.2u

## ESS\_OSC



## EMI

Close chip.



msi MICRO-STAR INT'L CO.,LTD.

File  
ES9016-2M/SABRE9601K  
Size  
Customer  
MS-16K41  
Date: Friday, November 04, 2016  
Sheet 40 of 66  
Rev 0A

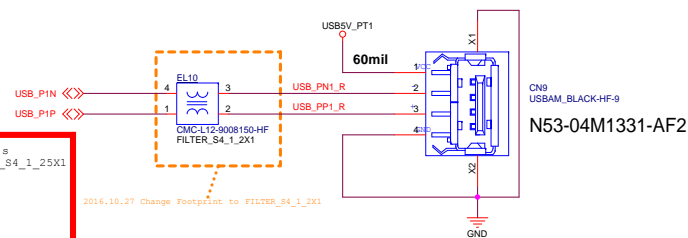


## USB2.0/Keyboard control

**I36-5478102-G07**

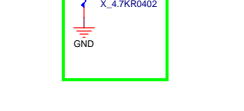
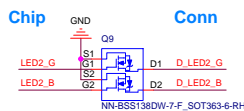
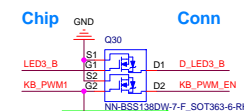
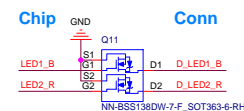
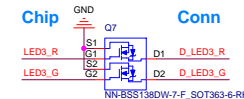
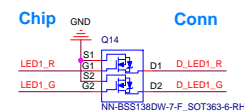
**G5478I1 MAX : 2.5A**

CMC-L12-9008150-HF(P/N : L12-  
Default Orcad library and fo  
are not match datasheet.



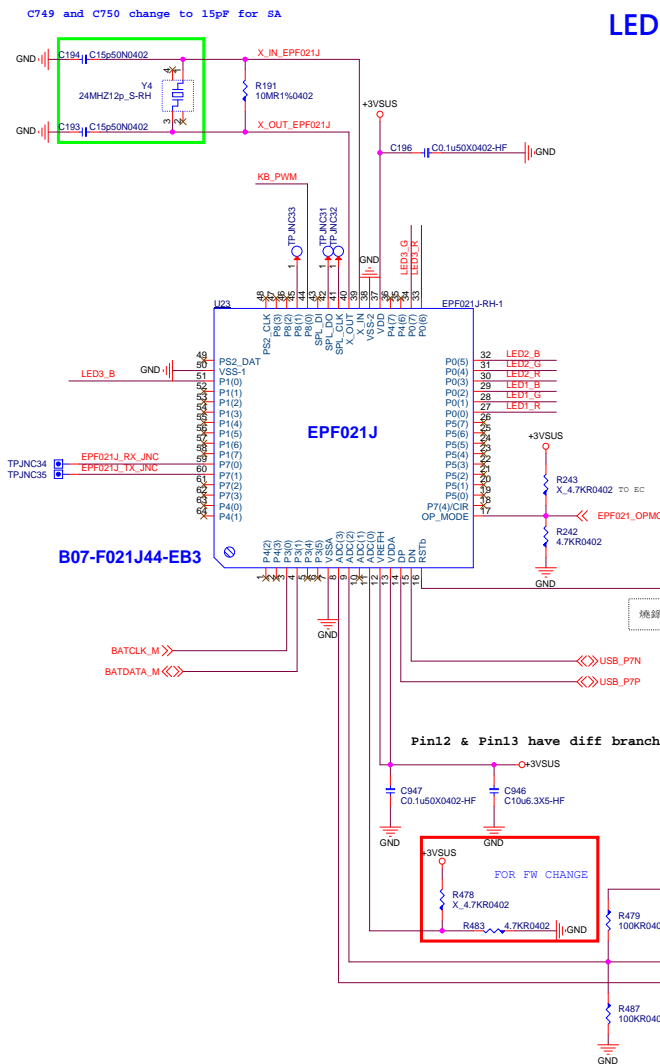
The schematic shows two horizontal lines representing USB pins. The top line is labeled 'USB\_PN1\_R' on the left, followed by 'C1031' and a capacitor symbol. To the right of the capacitor is 'X C10p50N0402', and further right is a ground symbol labeled 'G'. The bottom line is labeled 'USB\_PP1\_R' on the left, followed by 'C1029' and a capacitor symbol. To the right of the capacitor is 'X C10p50N0402', and further right is a ground symbol labeled 'G'.

EPF021J Sink current not enough, only using BSS138 (0.22A)



### 問題

The diagram shows a 5V regulator circuit. The input is connected to DIMM\_ON\_2V5 and KB\_PWM1. The output is connected to KB\_PWM1. The circuit includes a 3V3V\_S1US supply, a C923 capacitor, a C0.1u50X0402-HF capacitor, and a R457 resistor.



Pin12 & Pin13 have diff branch

FOR EM CHANGE

HP\_R\_ADC

電容配置位置 需 確認  
INRUCH CURRENT

40mH

5V\_SUSKB

5V\_SUS

KB\_PWM\_EN

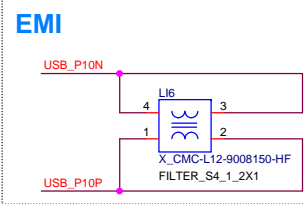
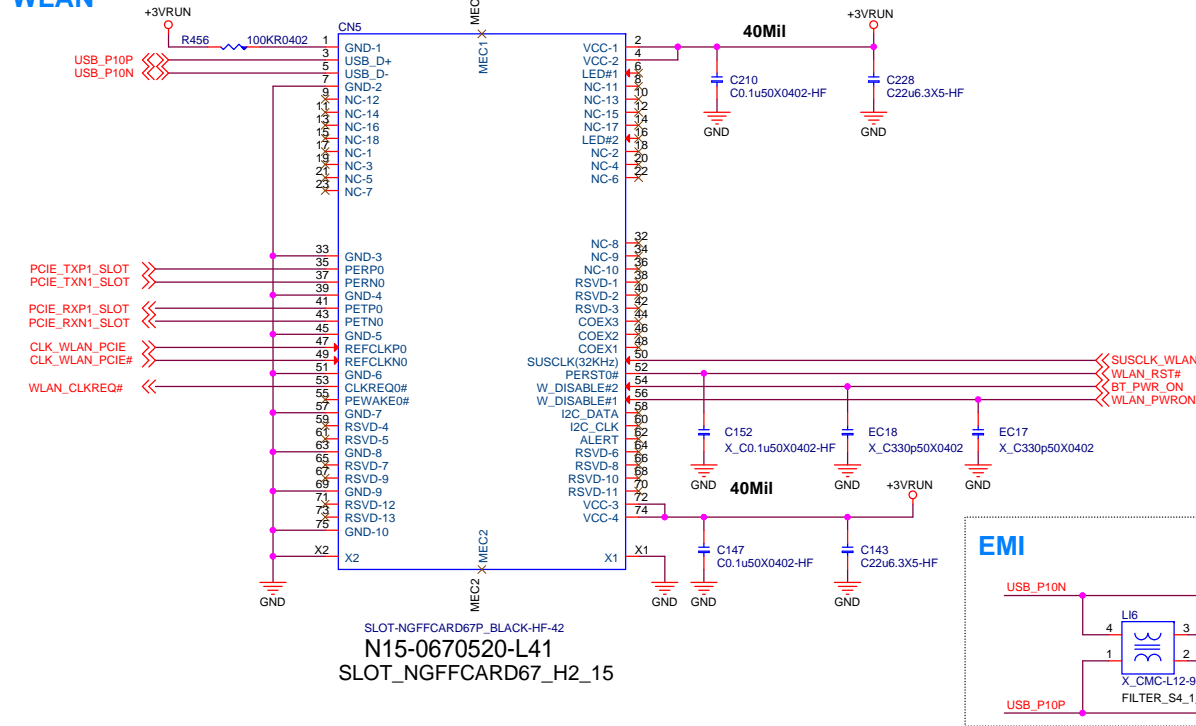
FCP3  
FPC12P-0.5PITCH\_BLACK-HF-1  
N5A-12F0330-A81  
掀蓋式

LED Keyboard Pin Define	
Pin 1	VCC_G
Pin 2	VCC_R
Pin 3	VCC_B
Pin 4	LED1_B
Pin 5	LED1_R
Pin 6	LED1_G
Pin 7	LED2_B
Pin 8	LED2_R
Pin 9	LED2_G
Pin 10	LED3_B
Pin 11	LED3_R
Pin 12	LED3_G



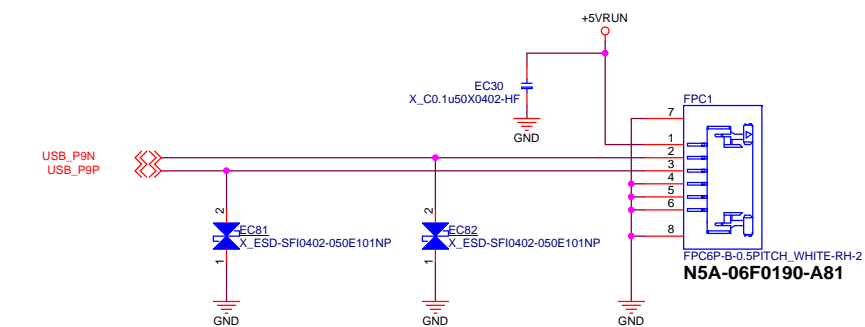
# WLAN /ClickPad/FP

## WLAN

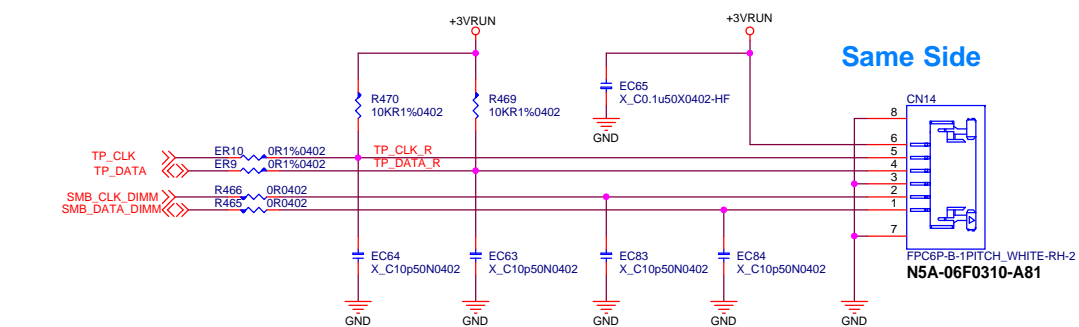


Pin 1	GND	Pin 2	3.3V
Pin 3	USB_D+	Pin 4	3.3V
Pin 5	USB_D-	Pin 6	LED1#
Pin 7	GND	Pin 8	Module Key
Pin 9	Module Key	Pin 10	Module Key
Pin 11	Module Key	Pin 12	Module Key
Pin 13	Module Key	Pin 14	Module Key
Pin 15	Module Key	Pin 16	LED2#
Pin 17	N/C	Pin 18	GND
Pin 19	N/C	Pin 20	N/C
Pin 21	N/C	Pin 22	N/C
Pin 23	Module Key	Pin 24	Module Key
Pin 25	Module Key	Pin 26	Module Key
Pin 27	Module Key	Pin 28	Module Key
Pin 29	Module Key	Pin 30	Module Key
Pin 31	Module Key		
Pin 33	GND	Pin 32	N/C
Pin 35	PERP0	Pin 34	N/C
Pin 37	PERN0	Pin 36	N/C
Pin 39	GND	Pin 38	Clink Reset (I 3.3V)
Pin 41	PETP0	Pin 40	N/C
Pin 43	PETN0	Pin 42	N/C
Pin 45	GND	Pin 44	N/C
Pin 47	REFCLKP0	Pin 46	N/C
Pin 49	REFCLKN0	Pin 48	N/C
Pin 51	GND	Pin 50	N/C (SUSCLK (32kHz) for DSx)
Pin 53	CLKREQ0#	Pin 52	PERST0#
Pin 55	PEWAKE0#	Pin 54	BT_EN (W_DISABLE2#)
Pin 57	GND	Pin 56	WLAN_EN (W_DISABLE2#)
Pin 59	N/C	Pin 58	N/C
Pin 61	N/C	Pin 60	N/C
Pin 63	N/C	Pin 62	N/C
Pin 65	N/C	Pin 64	Resever
Pin 67	N/C	Pin 66	N/C
Pin 69	N/C	Pin 68	N/C
Pin 71	N/C	Pin 70	N/C
Pin 73	N/C	Pin 72	3.3V
Pin 75	GND	Pin 74	3.3V

## Finger Print



## Click Pad

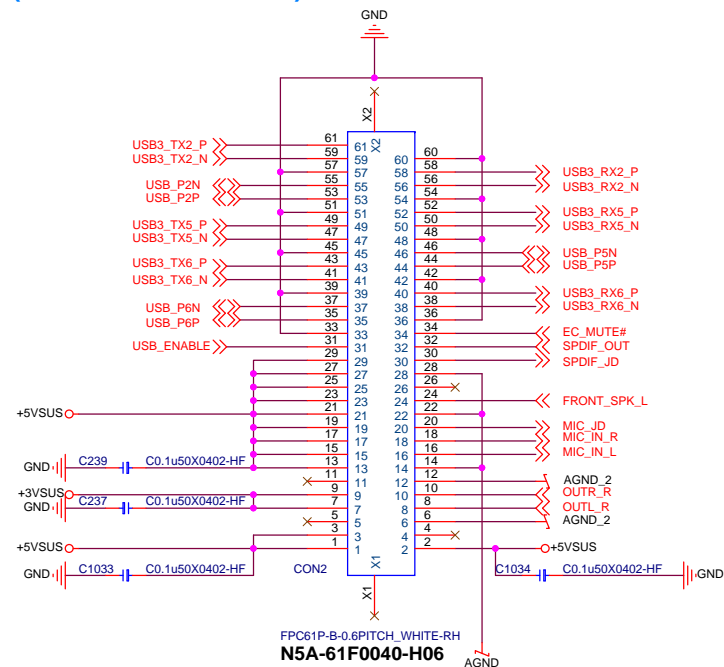


R473, R479 0ohm on part for TP SMBus function. 7/15

msi MICRO-STAR INT'L CO.,LTD.		
Title		
WLAN /ClickPad/FP		
Size	Document Number	Rev
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Date:	Friday, November 04, 2016	Sheet 42 of 66

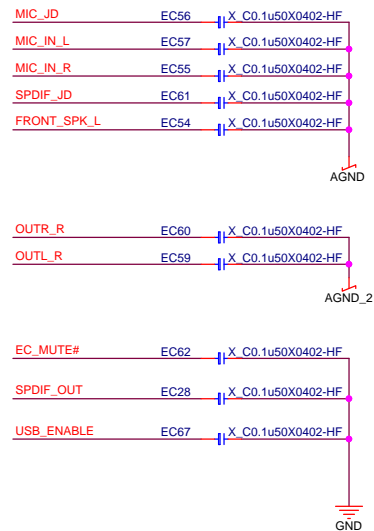


## (Audio CONN/USB3.0)

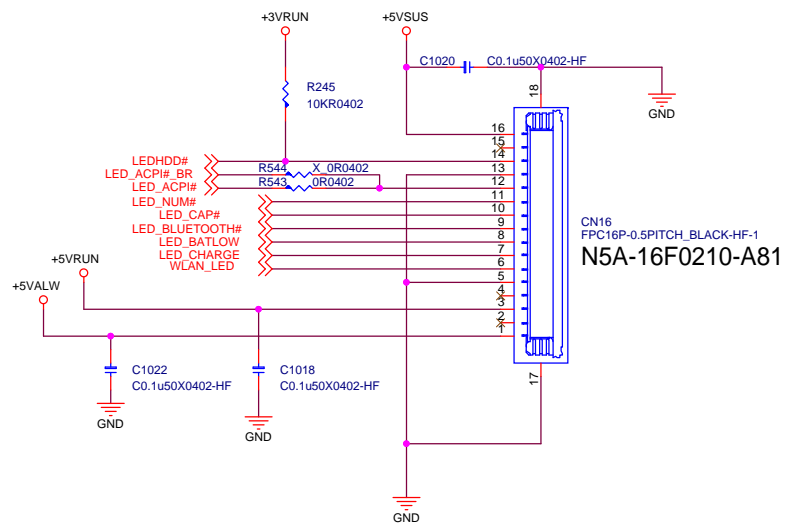


## BTB CONN

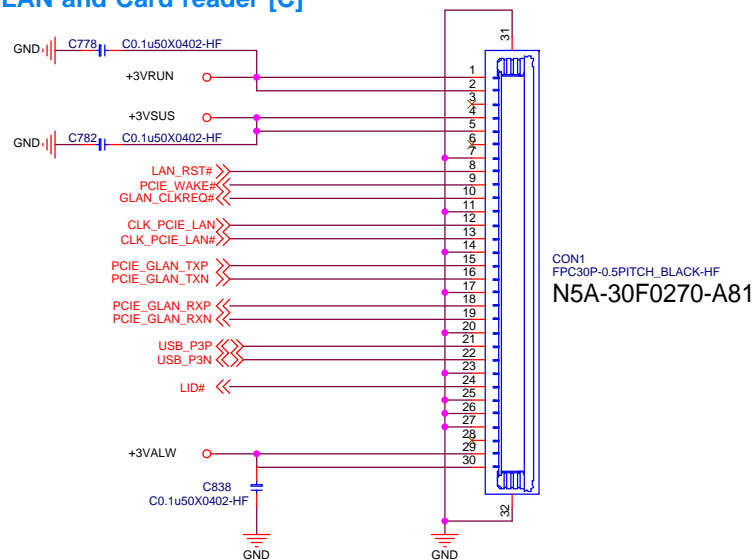
### EMI



## LED Board [B]

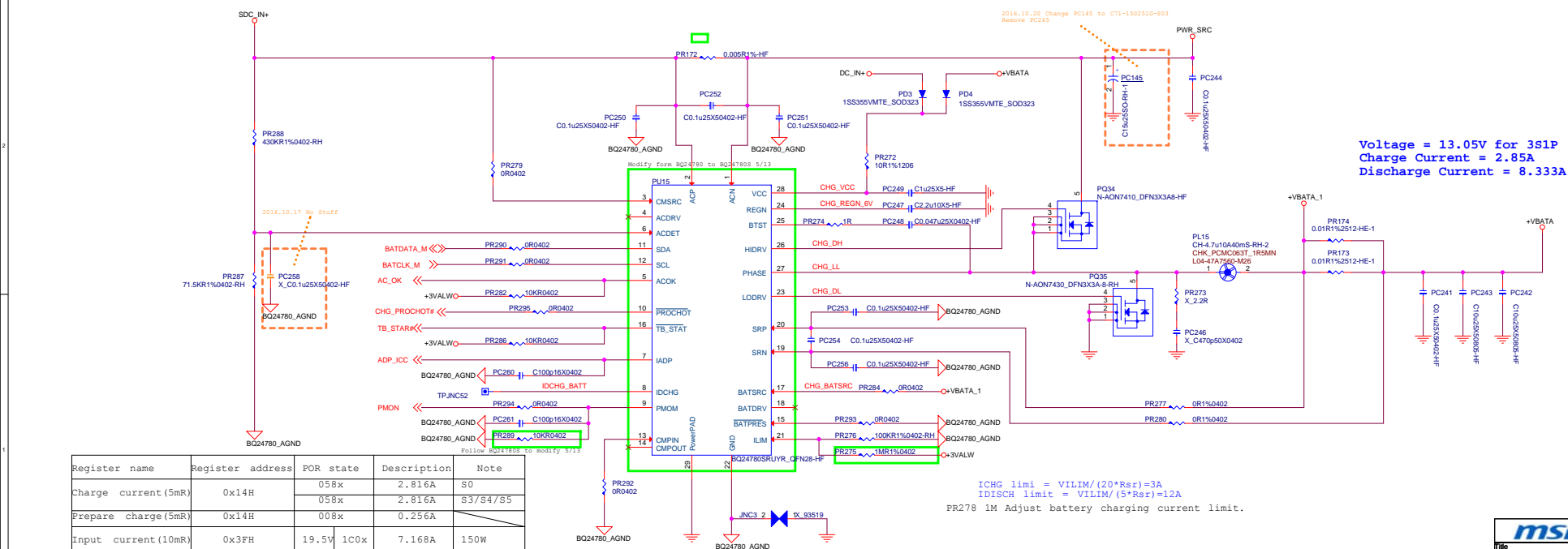
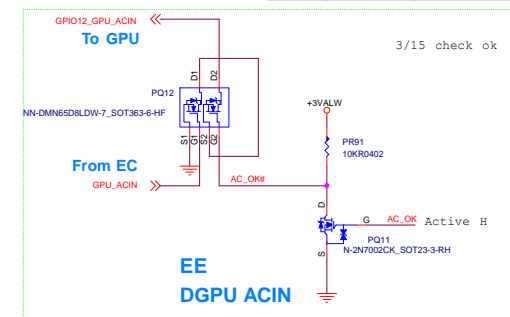
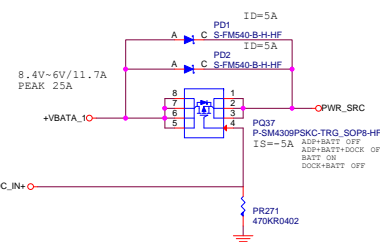
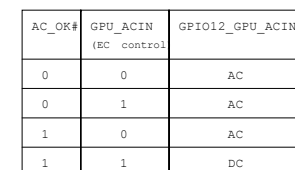


## LAN and Card reader [C]





N54-03F0751-S56  
9.5A/20V



Follow BQ24T808				
Register name	Register address	FOR state	Description	Note
Charge current (5mR)	0x14H	058x	2.816A	S0
		058x	2.816A	S3/S4/S5
Prepare charge (5mR)	0x14H	008x	0.256A	
Input current (10mR)	0x3FH	19.5V 1C0x	7.166A	150W
Charge voltage	0x15H	330x	13.056V	3S1P
Discharge current (5mR)	0x39H	06xx	3.072A	BOOST current

```

        ICHG limi = VILIM/(20*Rsr)=3A
        IDISCH limit = VILIM/(5*Rsr)=12A
PR278 1M Adjust battery charging current limit.

```

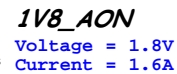
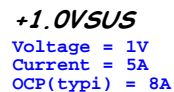
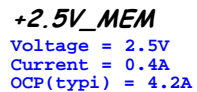














Follow Intel VTT Tools test result to adjust 5/13

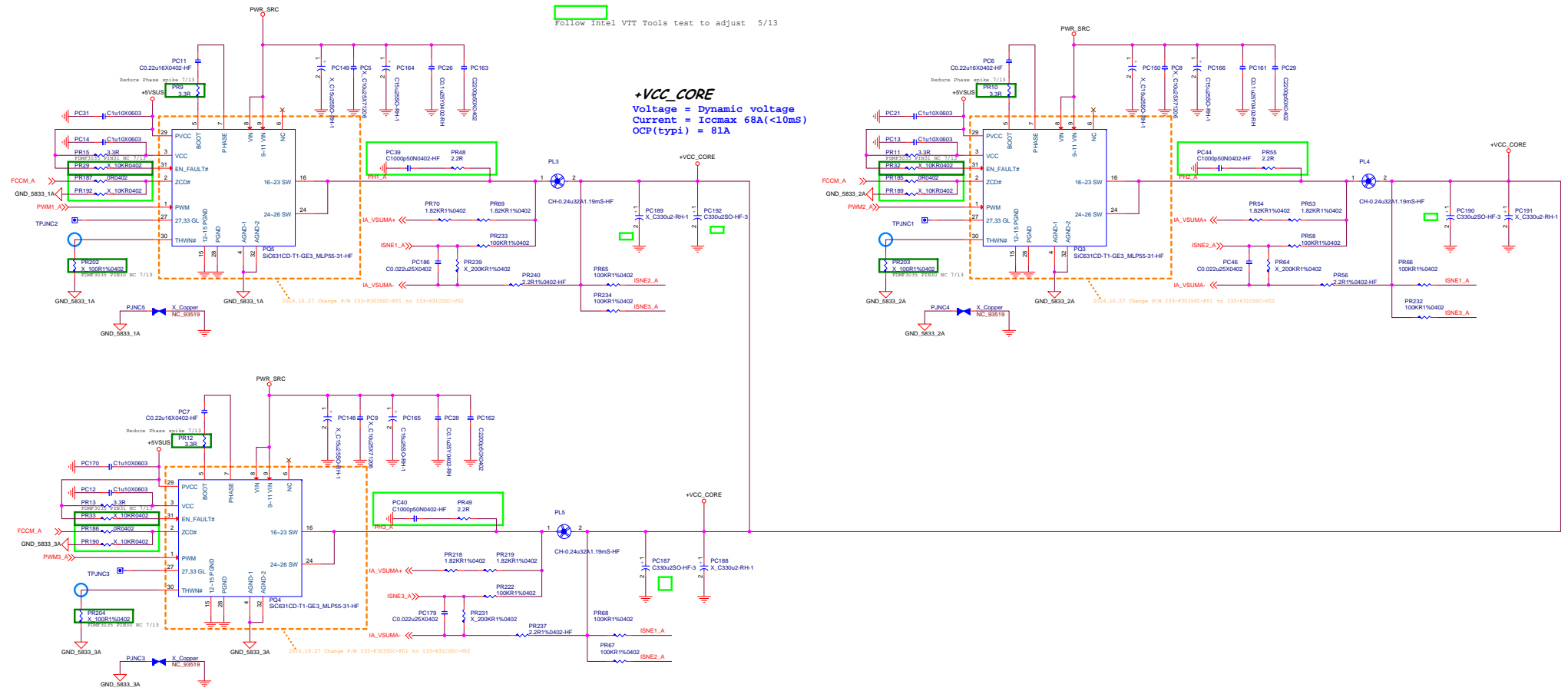


PROG1	L10KR	/boot=UV, Selw rate=30mV/us, VR_A=IA, VR_B=GT, VR_C=SA
PROG2	71.5KR	IMAX VR_A=70A, VR_A PS11=1PH
PROG3	20.5KR	IMAX VR_B=60A, DROOP VR_B Active
PROG4	182KR	DROOP VR_A Active, DROOP VR_C Active, VR_A VR_B Frequency=750kHz
PROG5	78.7KR	IMAX VR_C=12A, Frequency=583KHz

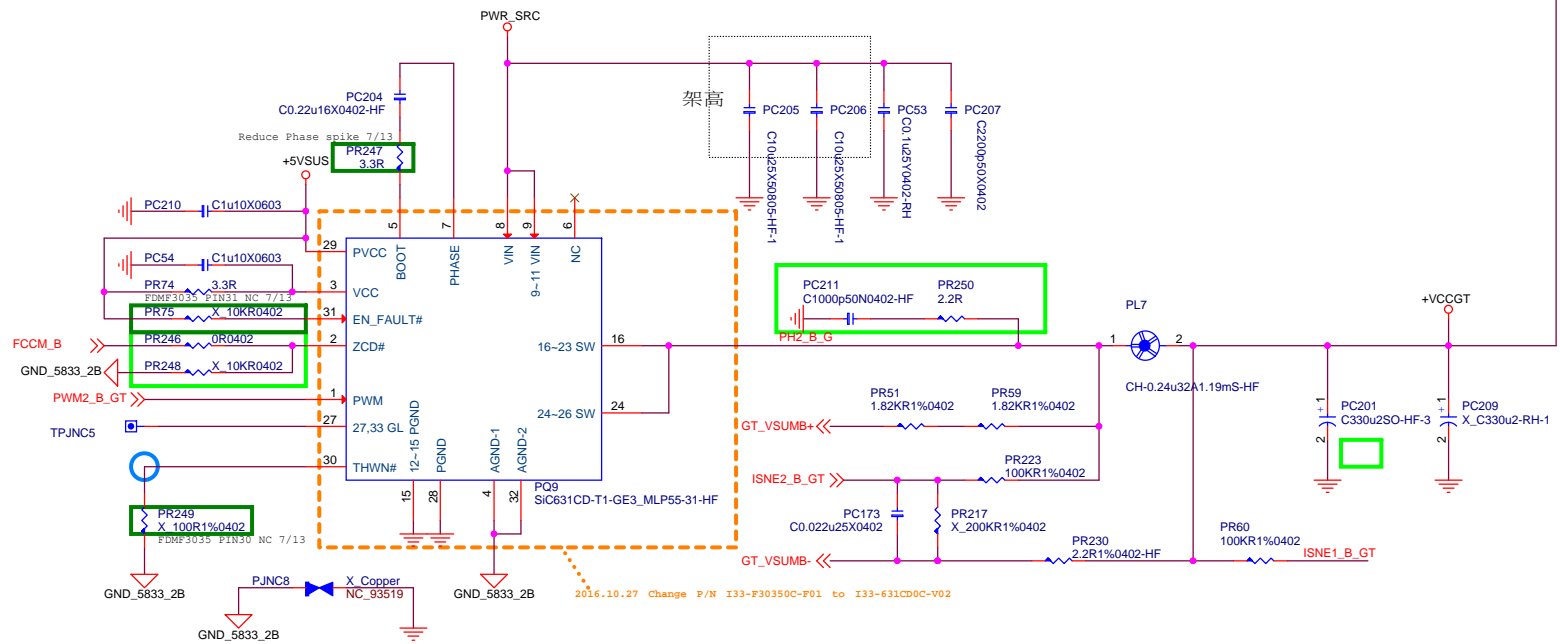
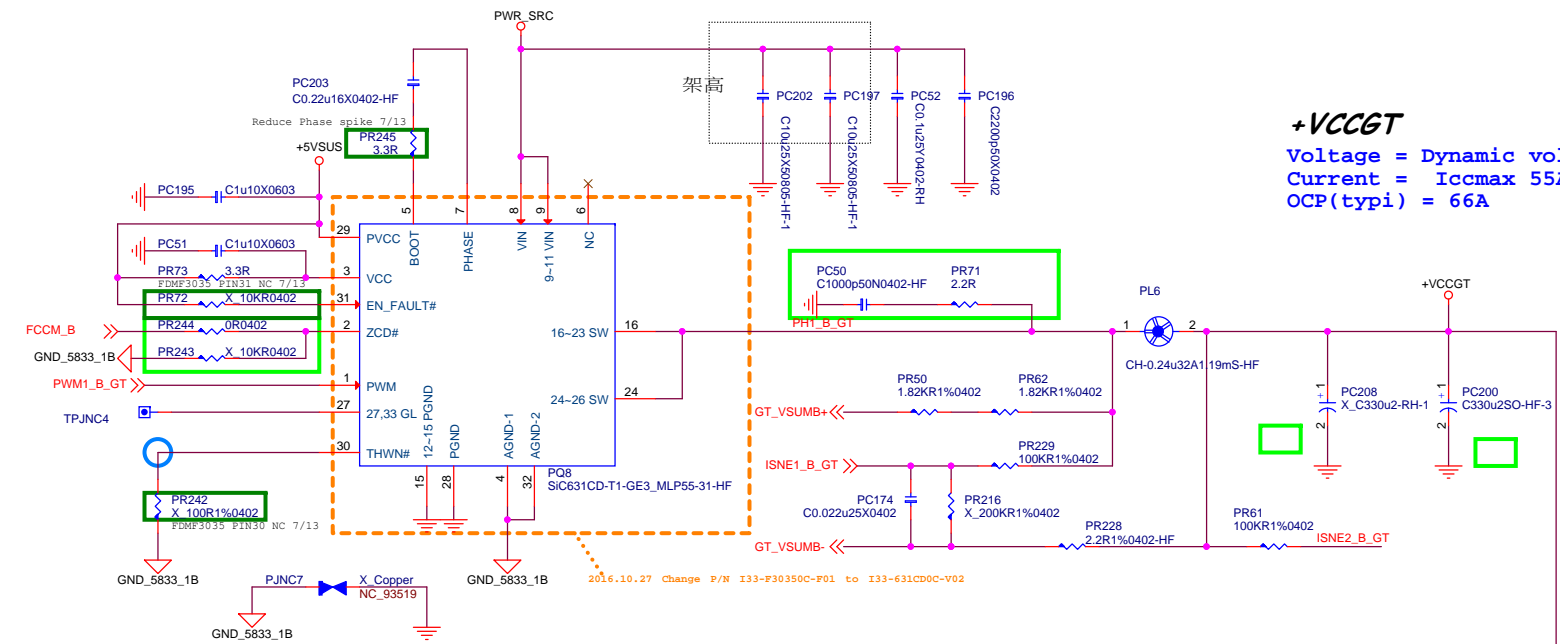


Follow Intel VIT Tools test to adjust 5/13

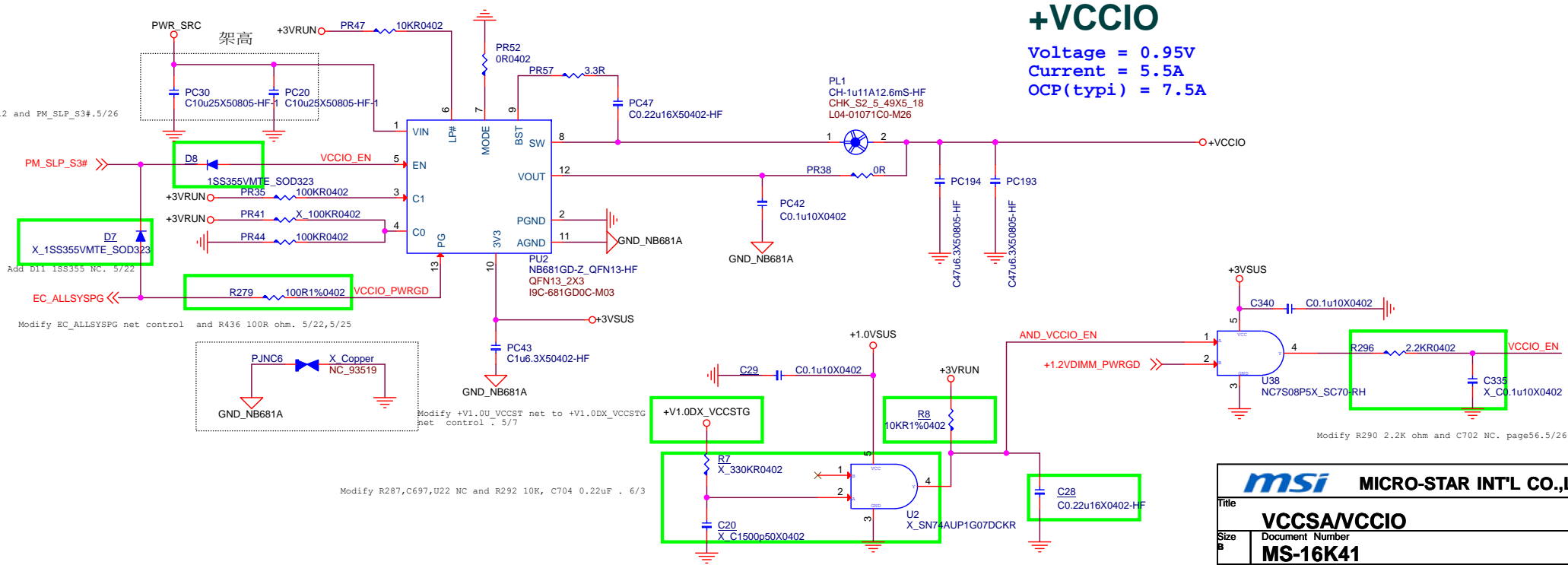
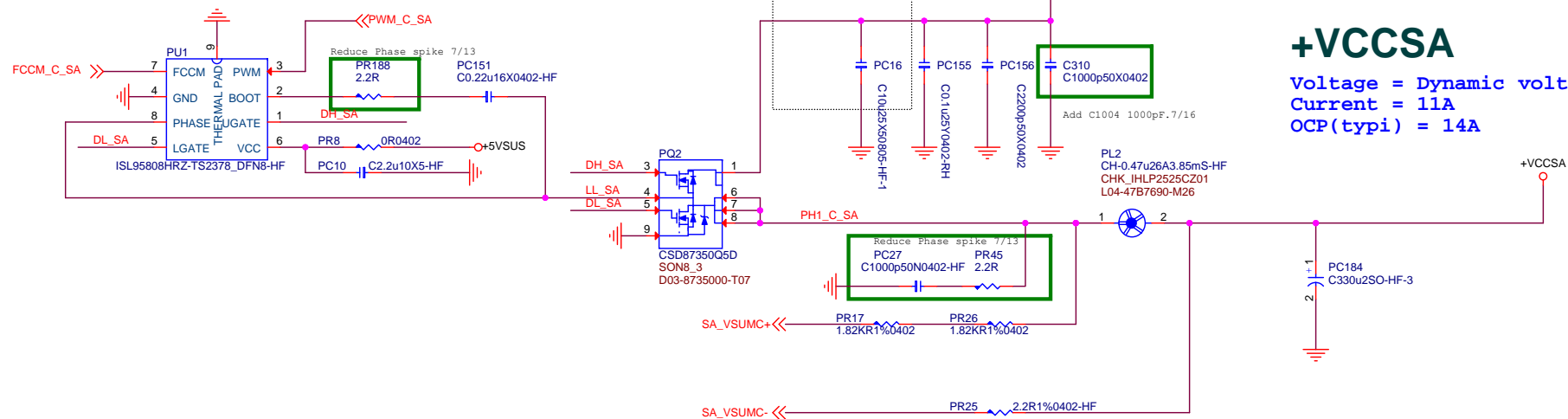
**+VCC\_CORE**  
Voltage = Dynamic voltage  
Current = Iccmax 68A(<10ms)  
OCP(typi) = 81A











<b>msi</b> MICRO-STAR INT'L CO.,LTD.	
Title <b>VCCSA/VCCIO</b>	
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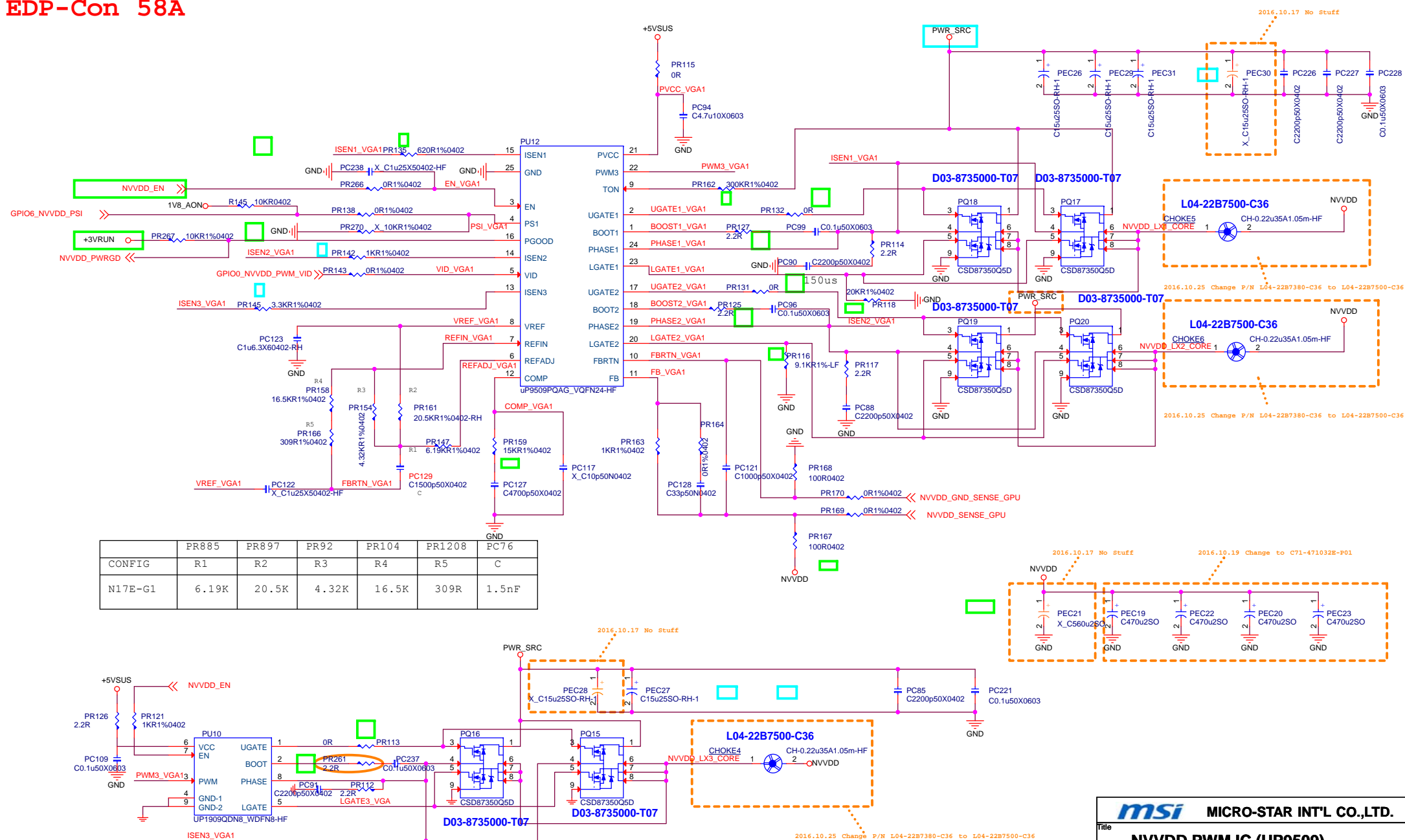






EDP-Peak 101A  
EDP-Con 58A

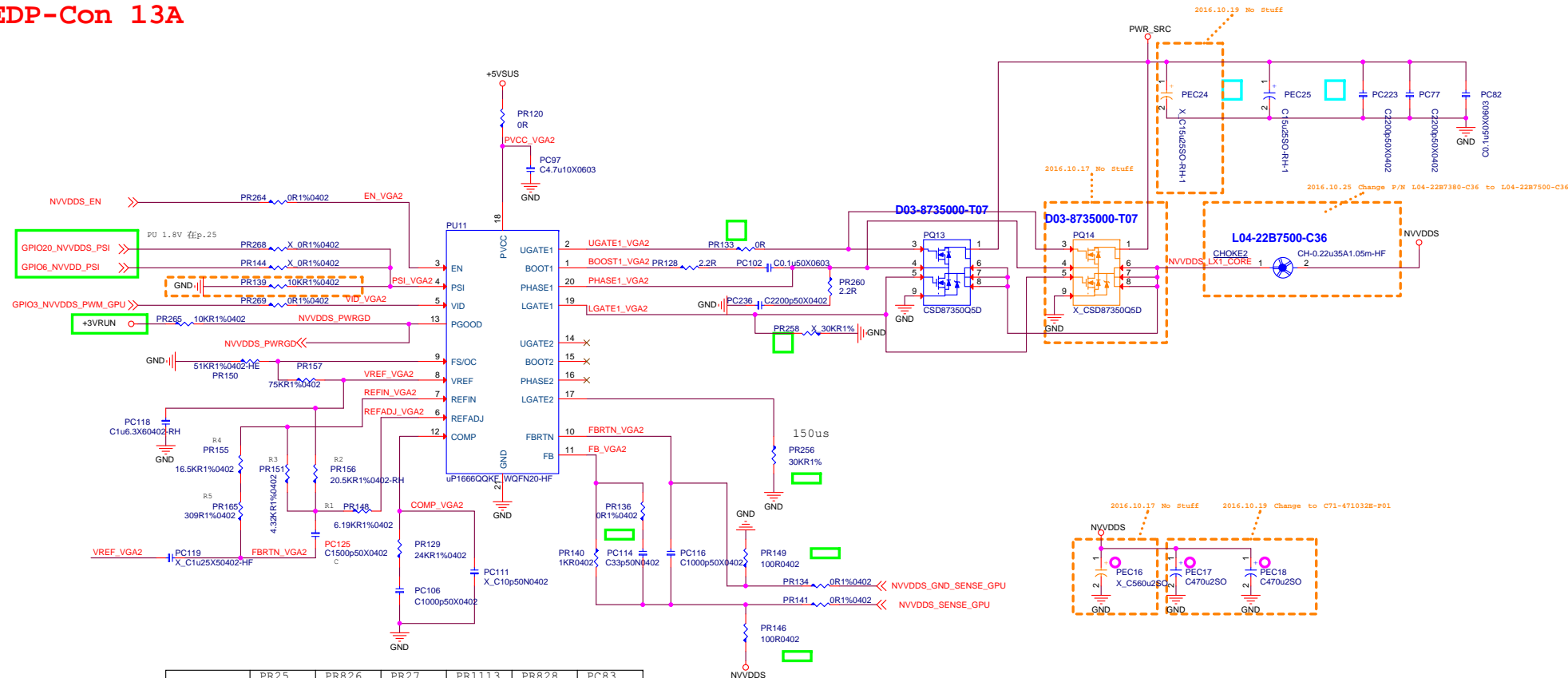
VBoot:0.8V  
Vmin:0.3V / Vmax:1.3V





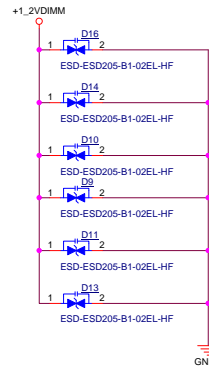
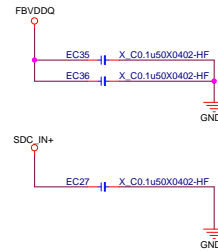
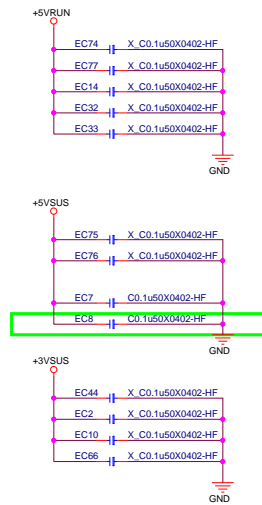
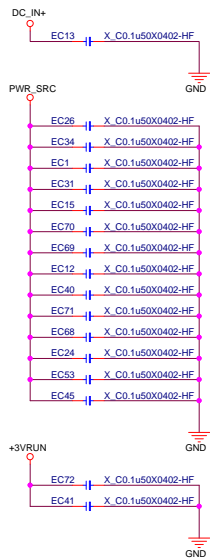
EDP-Peak 18A  
EDP-Con 13A

VBoot:0.8V  
Vmin:0.3V / Vmax:1.3V

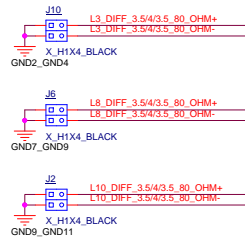


	PR25	PR826	PR27	PR1113	PR828	PC83
CONFIG	R1	R2	R3	R4	R5	C
N17E-G1	6.19K	20.5K	4.32K	16.5K	309R	1.5nF

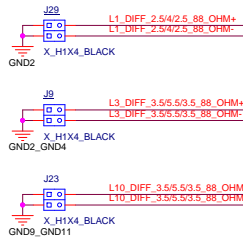




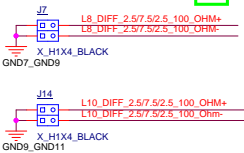
### 80 OHM / CLK/WCK



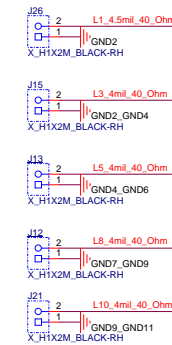
### 88 OHM / DDR4 CLK/DQS



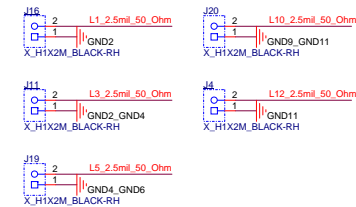
### 100 OHM / LAN



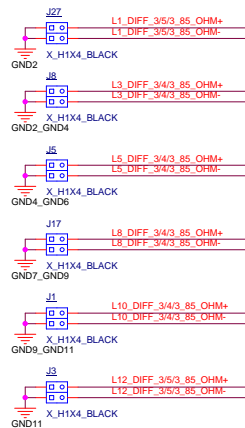
### 40 OHM / DDR4 CTRL



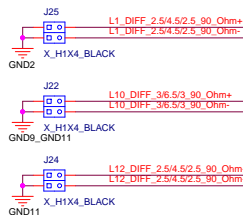
### 50 OHM / NORMAL / DDR4 DQ



### 85 OHM / SATA / PCH PCIE/ EDP USB /HDMI/DP/DMI/CLK/PEG



### 90 OHM / Alpine Ridge

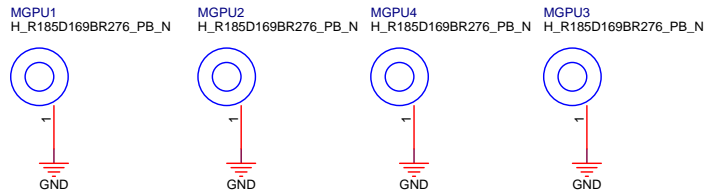


### 95 OHM / LAN

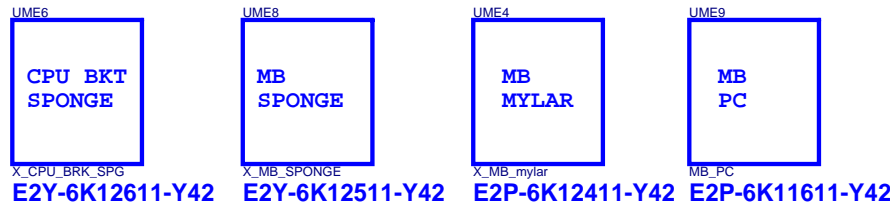
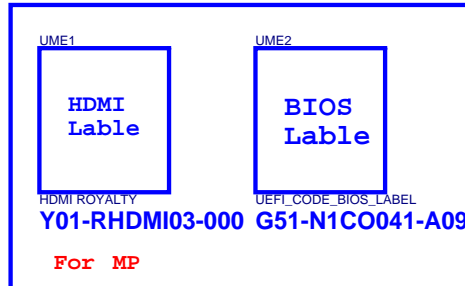
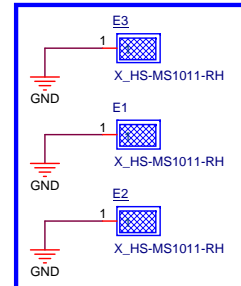
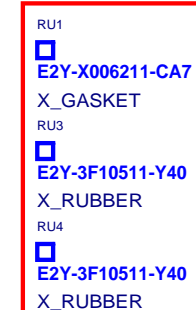
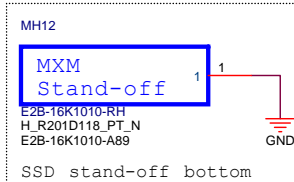
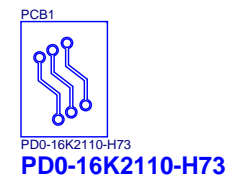
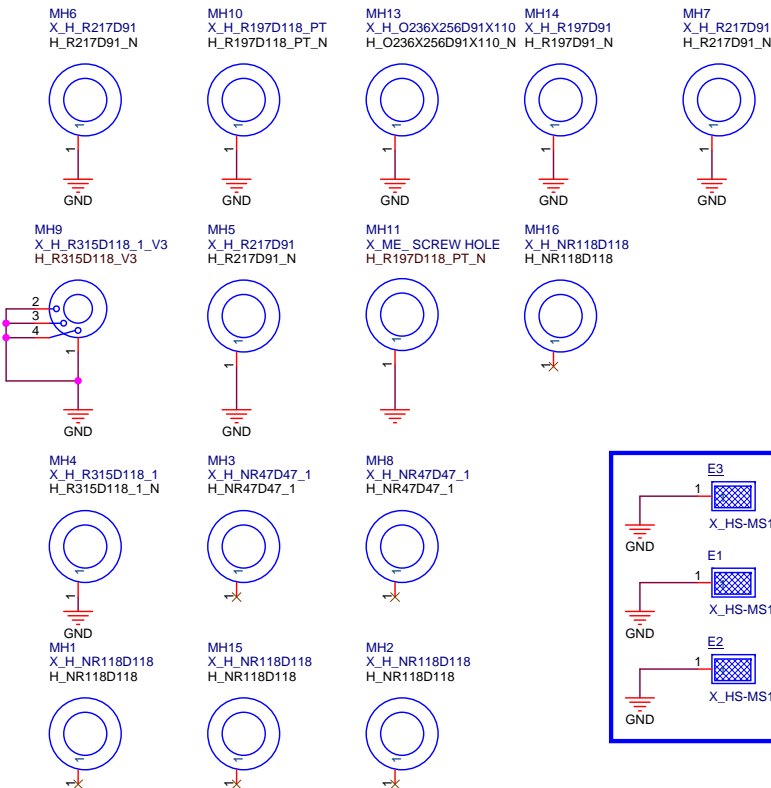
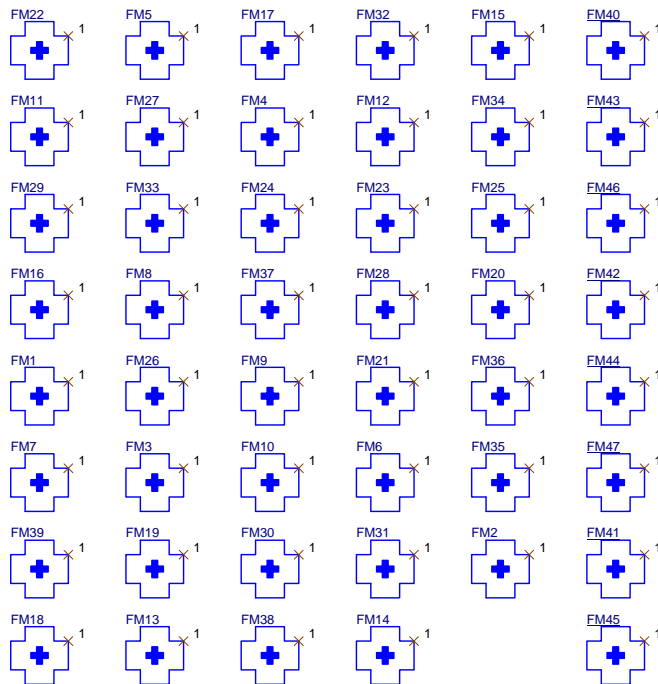
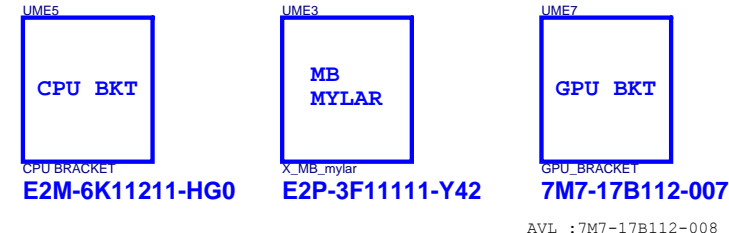
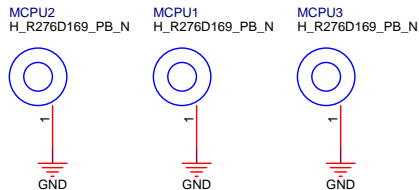




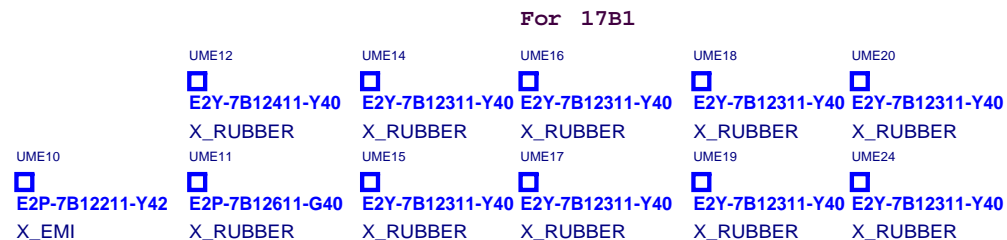
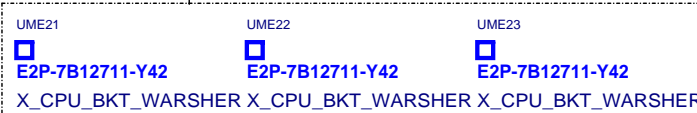
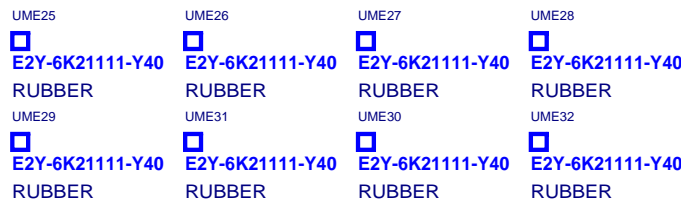
## dGPU Holes



## CPU Holes



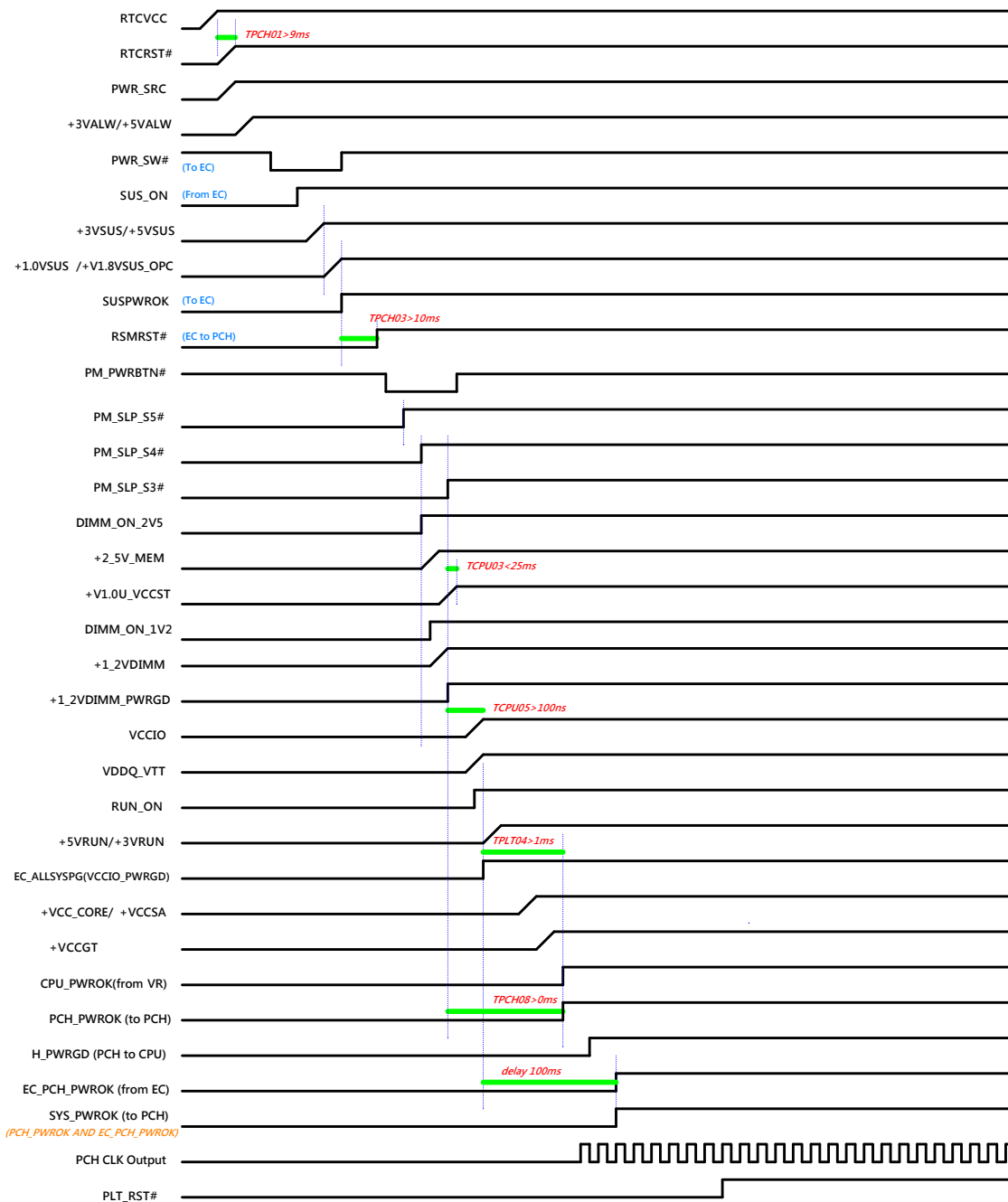
For 16K2  
RU2  
E2M-3570611-G40  
MECH





# Power on Sequence

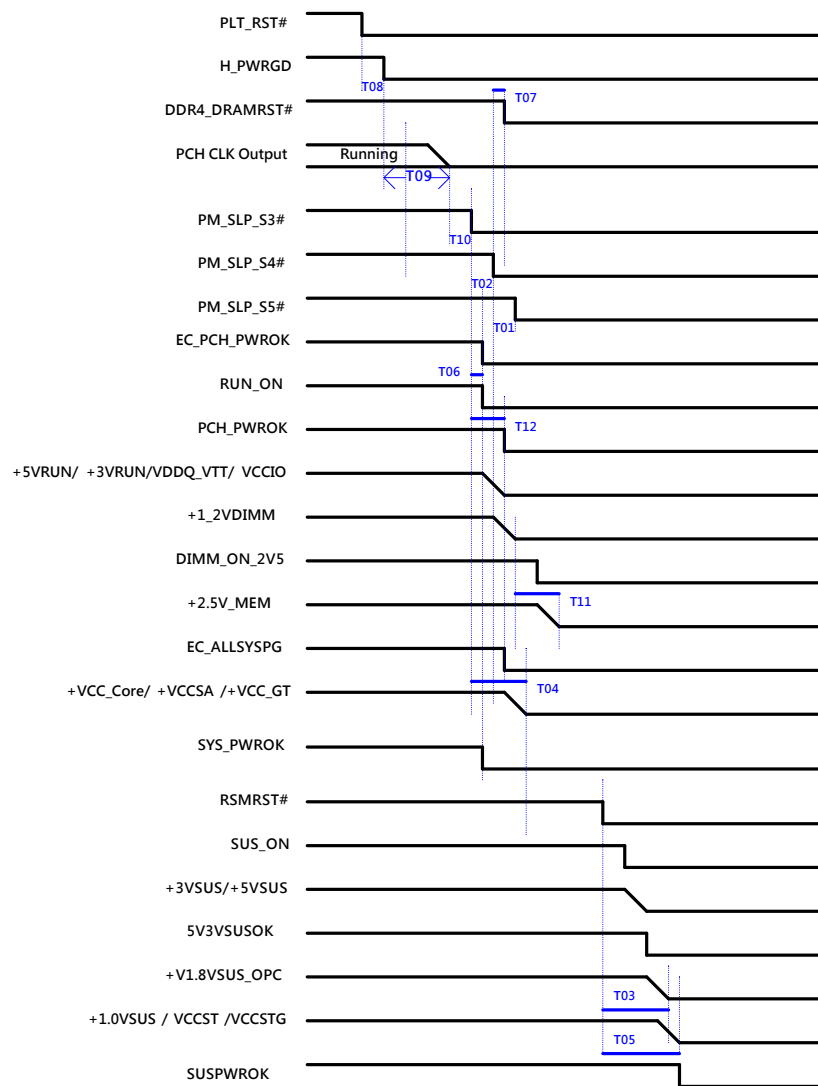
G3 -> S0





# Power down Sequence

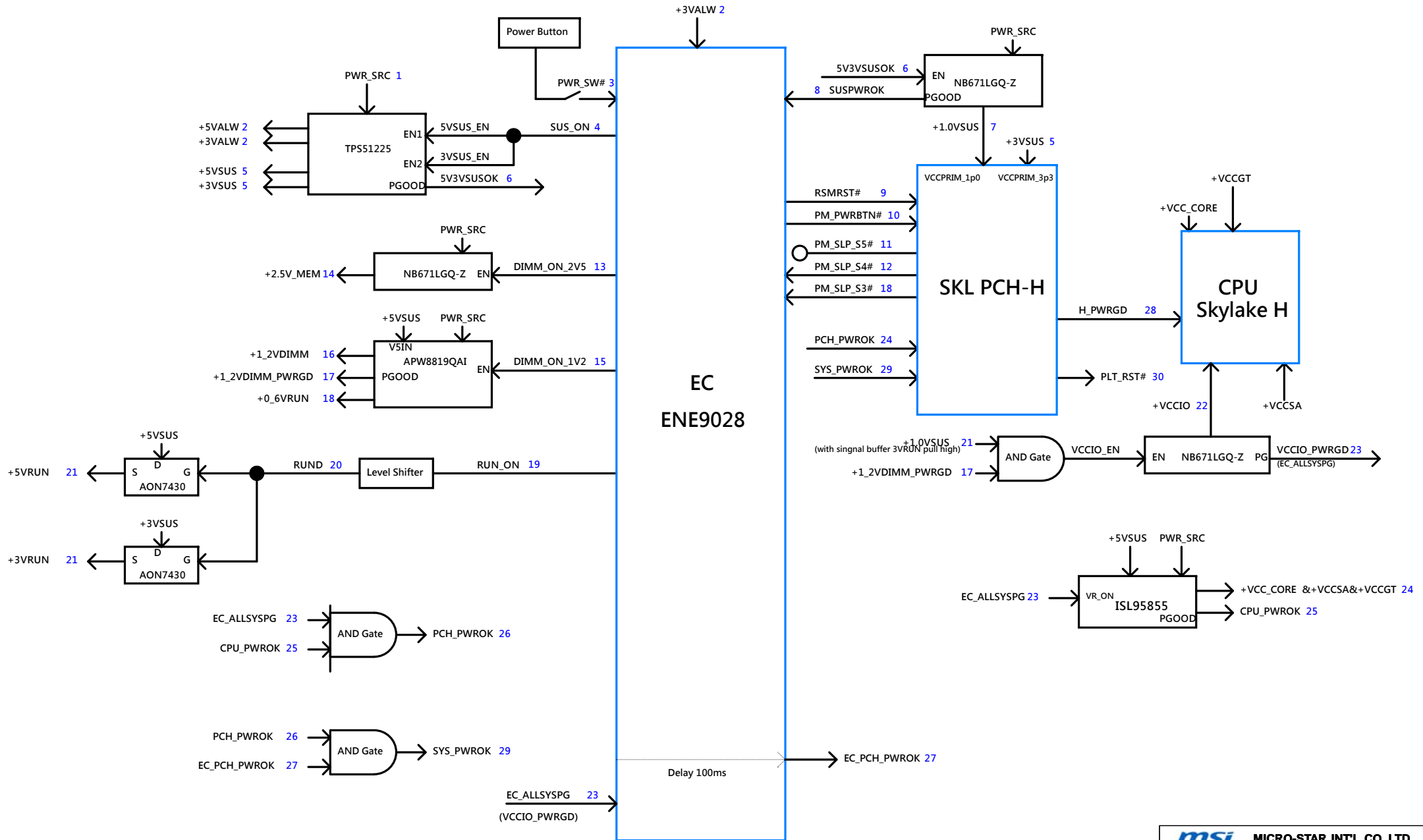
S0 -> G3



	MIN	MAX	Units	Description
T01	30		us	SLP_S5# assertion to SLP_S4#
T02	30		us	SLP_S4# assertion to SLP_S3#
T03	1		us	RSMRST# asserting to VccPRIM dropping 5% of nominal value
T04		500	ms	SLP_S3# assertion to VCC, VCCGT, VCCIO and VCCSA rails completely off.
T05	1		us	RSMRST# asserting to VccPRIM dropping 5% of nominal value
T06		1	us	SLP_S3# assertion to VCCIO VR disabled
T07	-100		ns	DDR_RESET# assertion to SLP_S4# assertion
T08	30		us	PLTRST# assertion to PROCPWRGD deassertion
T09	10		us	PROCPWRGD de-assertion to CLKOUT_BCLK turning OFF.
T10	1		us	CLKOUT_BCLK turning OFF to SLP_S3# assertion
T11	30		ms	VDDQ ramped down to VPP ramp down
T12	0		ms	SLP_S3# assertion to PCH_PWROK deassertion



# MS-16K2 Power on Block Diagram

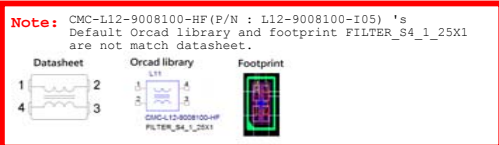
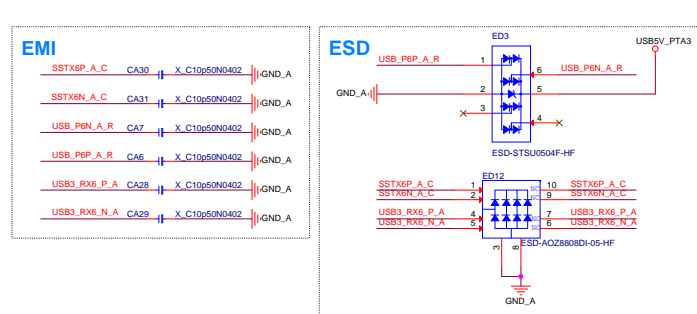
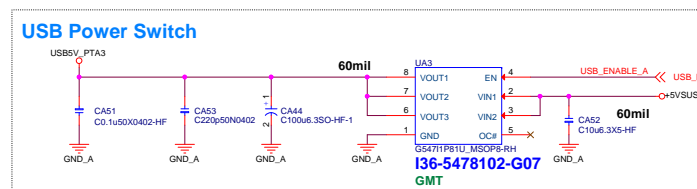
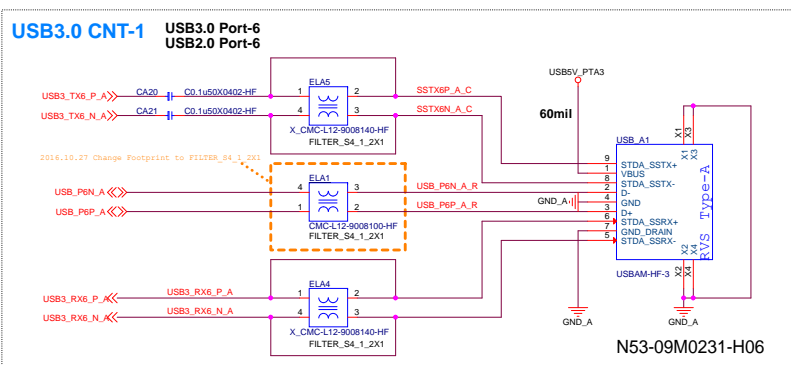
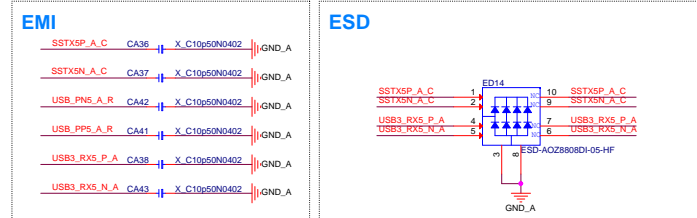
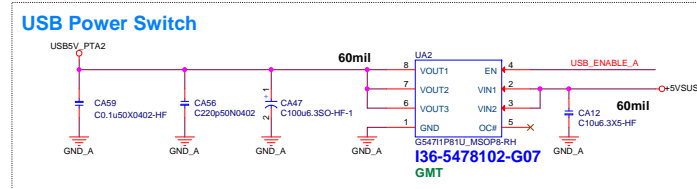
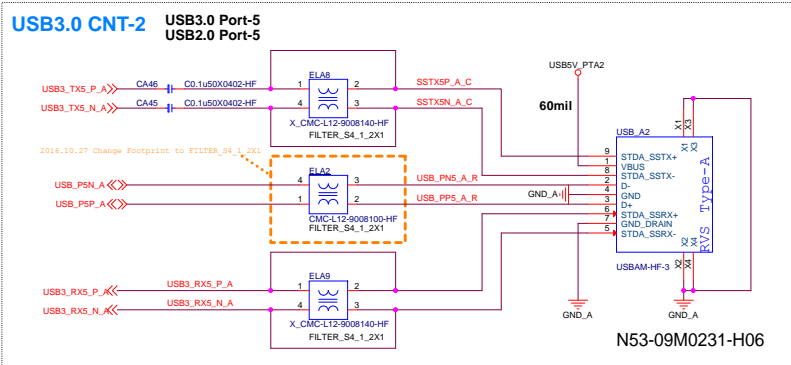
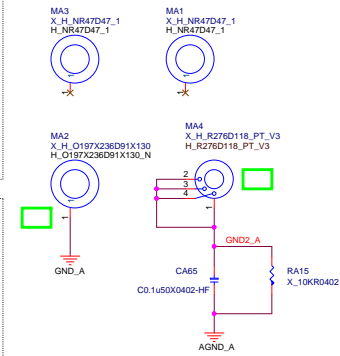
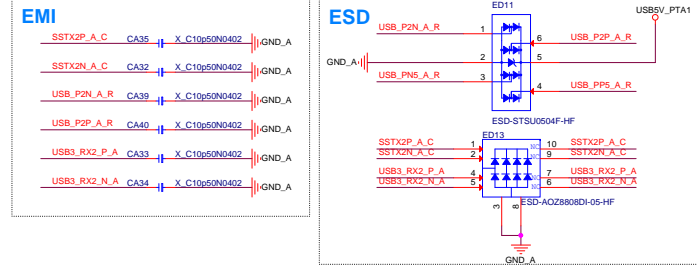
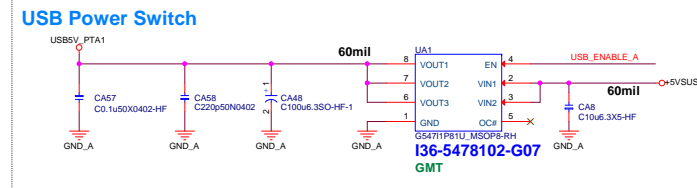
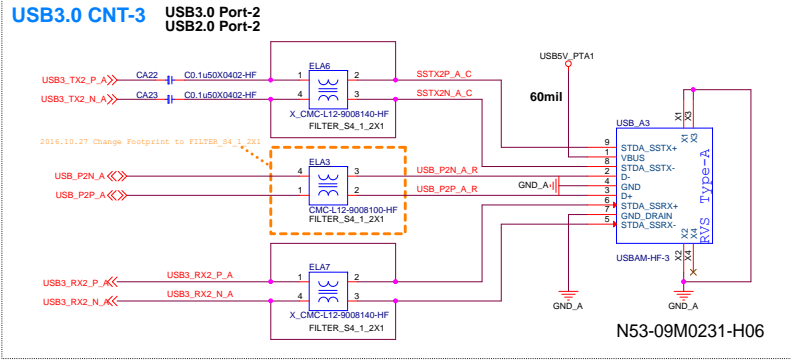






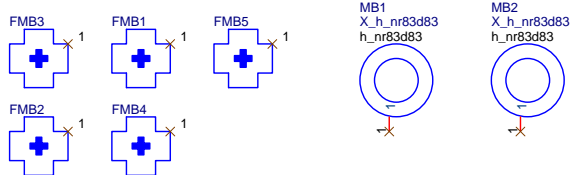
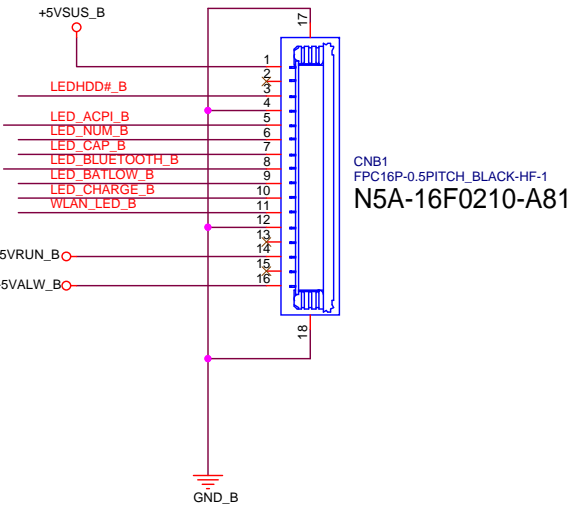
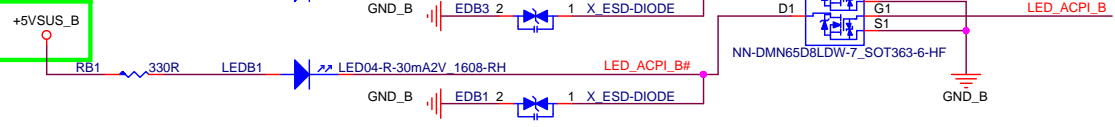
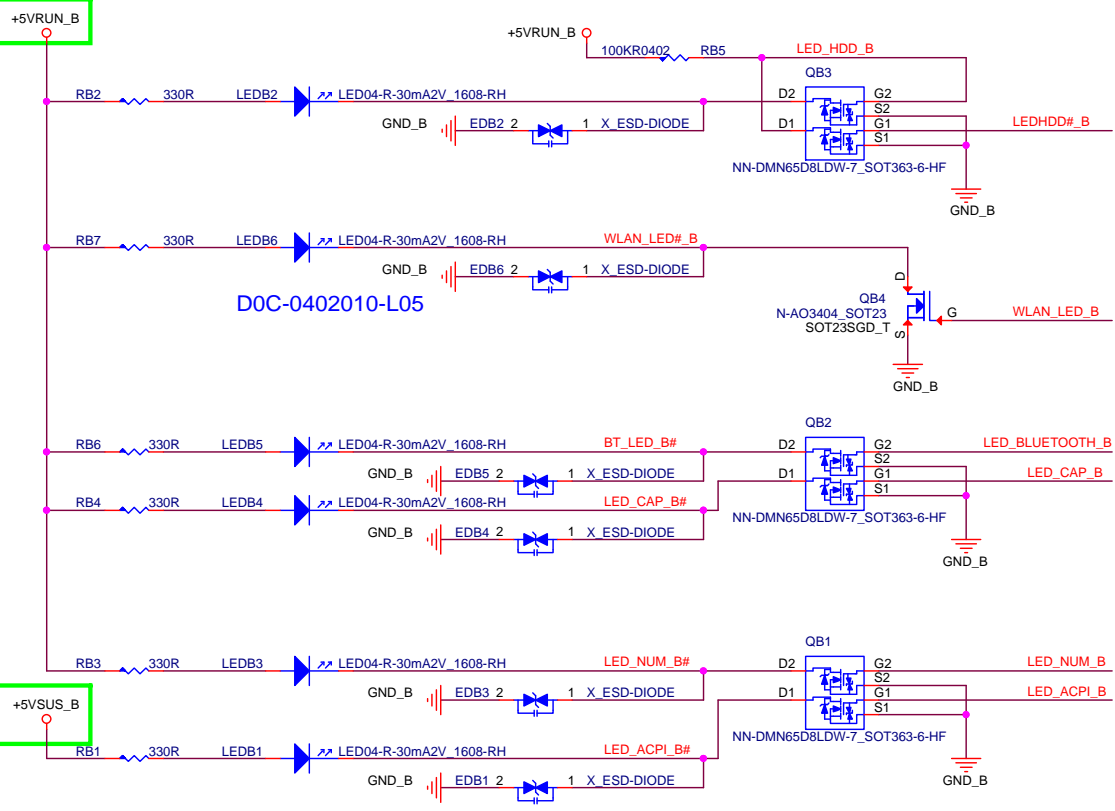
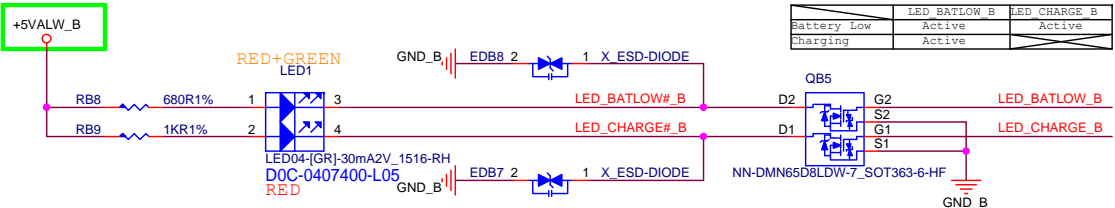
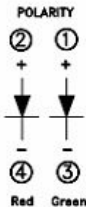


# [A] USB3.0 CNT-1/-2/-3

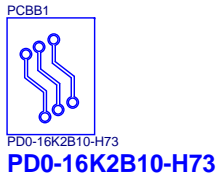




	LED BATLOW_B	LED CHARGE_B
Battery Low	Active	Active
Charging	Active	



Hannstar: P30-14A1A0B-H73  
TRIPOD: P30-14A1A0B-T53



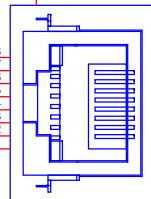
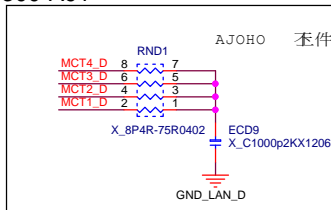
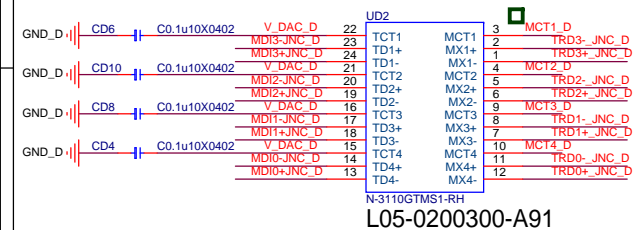
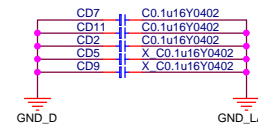
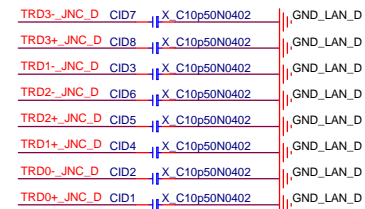
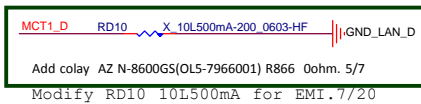
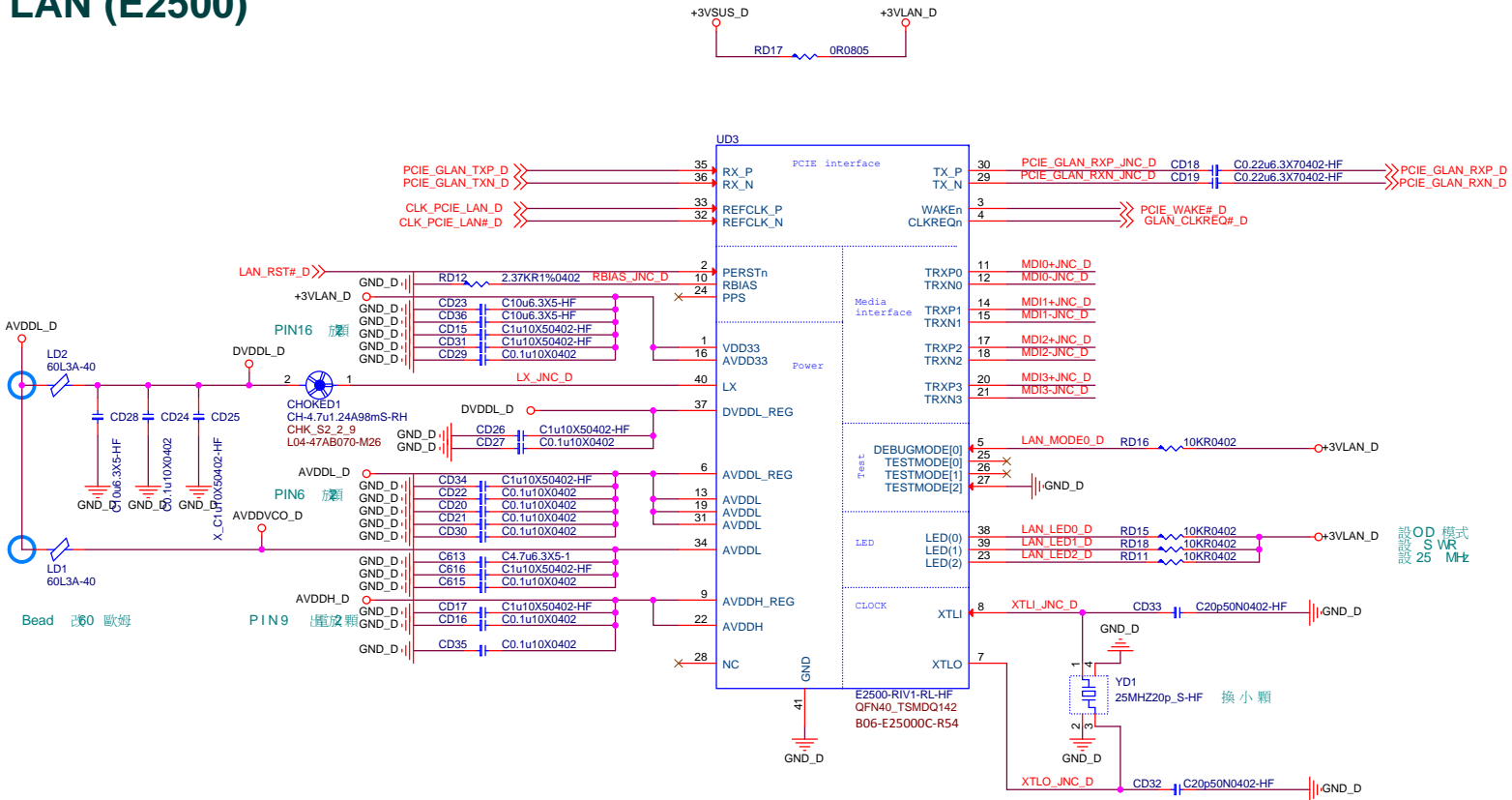
msi MICRO-STAR INT'L CO.,LTD.		
Title [B] LED		
Size	Document Number	Rev
MS-16K4B		0A
Date:	Friday, November 04, 2016	Sheet 62 of 66







## LAN (E2500)

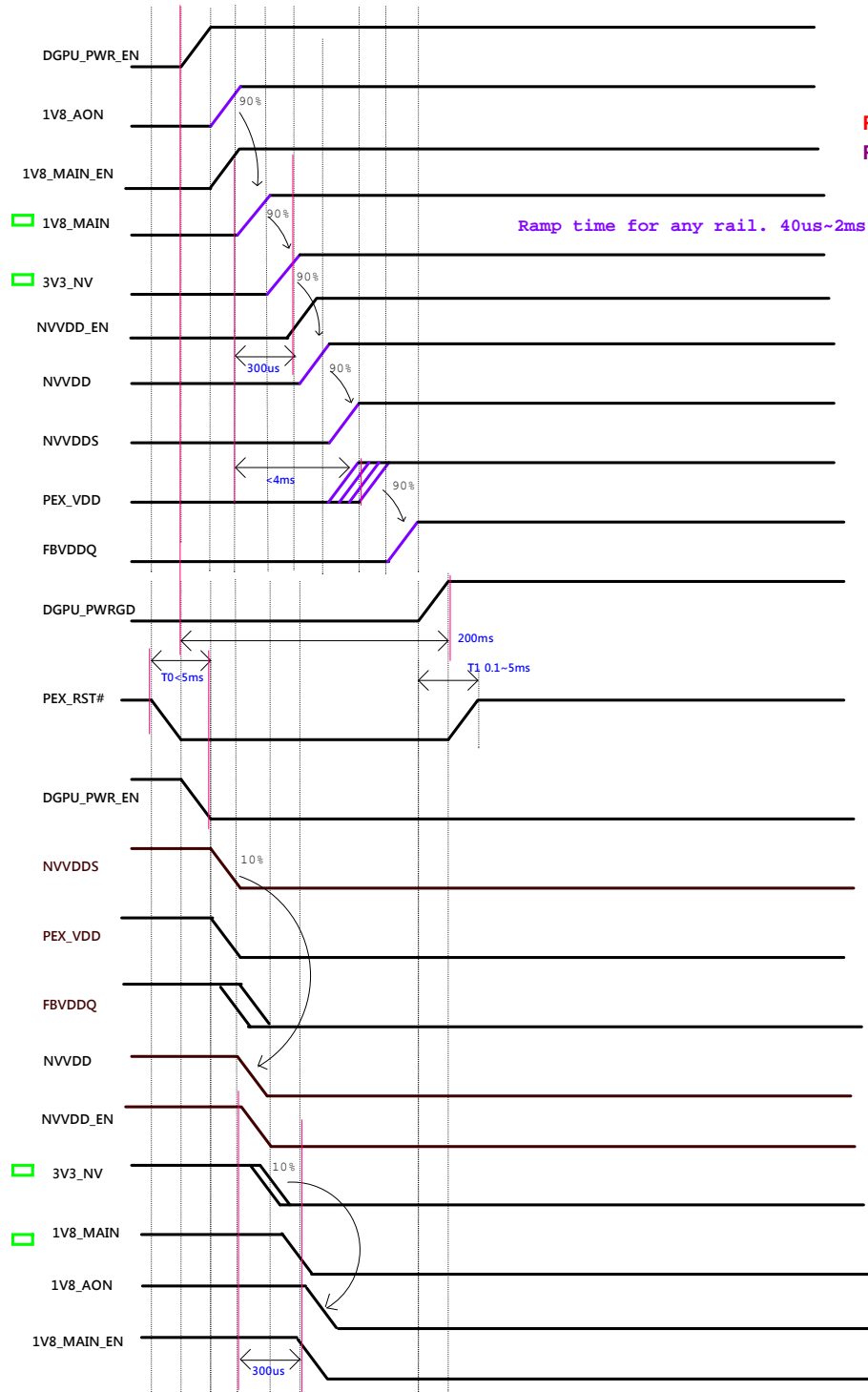


CND2  
LAN-RJ45-HF-4  
N55-08F0691-AF2

Change CN6 PN. 7/13.



# GPU Sequence




Power on = 1V8\_AON -> 1V8\_MAIN -> 3V3\_NV -> NVDD -> NVDDS/PEX\_VDD -> FBVDDQ -> DGPUPWRGD  
 Power off= DGPUPWREN->(NVVDDS->PEX\_VDD->FBVDDQ)->(NVVDD->3V3\_NV)->1V8\_MAIN->1V8\_AON



0B

## History

DATE	PAGE	DESCRIPTION	DATE	PAGE	DESCRIPTION	DATE	PAGE	DESCRIPTION
0217	60, 61	1. REMOVE CHOKE3, PR124, PC98, PR122, PC230, PR257 NVVDDS 2 概相	0311	55, 56 57	1. Vcore PC182 → 680 pF (C11-6811812-W08) PC189 → NC PR215 → 95.3kohm (R11-9532T12-W08) PR46 → 3kohm (R11-0302T12-W08)  Vgt PR182 → 84.5kohm (R11-8452T12-W08) PC15 → 470 pF (C11-4712012-T04) PC208 → NC PR199 → 3.16kohm (R11-3161T12-W08)  Vsa PR43 → 88.7kohm (R11-8872T12-R01) PC172 → 1200 pF (C11-1222832-W08)  NVVDDS P R 2 5 8 不件 P R 2 5 6 上件	0311	60	1. PR116 改 1K R11-0912T23-W08 (For ramp up time) 2. PR142, PR135 改 620ohm R11-0621T12-W08 3. PR162 改 200K R11-0304T12-W08 4. PR159 改 5K R11-0153T12-W08 5. PR118 改 20K R11-0203T12-R01 6. PR145 改 510ohm R11-0511T12-W08 7. PR129 改 4K R11-0243T12-W08
	63	1. REMOVE E2					69	1. CHANGE LED R TO 330R
0219	47	1. Change Y3 PN				0412	38	1. R116, R120 NO STUFF
	54	1. PR92 CHANGE TO 3.92KOhm 2. PR84 CHANGE TO 300KOhm					63	1. UME4 CHANGE E2P-6K12411-Y42 2. ADD UME6, UME8, UME9
0301	30	1. ADD R549 1KOhm				0415	70	1. ADD UMEC1
	30	1. CIRCUIT CHANGE TO PIN2						<b>1.0</b>
0302	35	1. CHANGE U12 PN , VCC CHANGE TO 1.8V	0314	39, 48	1. CHANGE EL9, EL10 FOOTPRINT	0419	44	1. R545 STUFF FOR PCIE SSD
0304	67	1. LA1 NO STUFF		43	1. CN11 PIN2&PIN3 SWAP 2. FPC2 PIN3&PIN4 SWAP	0420	70	1. ADD UMEC2
0307	51	1. PR172 CHANGE TO 0.005Ohm					63	2. REMOVE RU1
	34	1. CN10 CHANGE +/- , CHANGE BAT2 PN				0418	30	1. ADD R550, C1041 AND STUFF, U44 NO STUFF
	59, 60 , 61	1. CHOKE1, 2, 4, 5, 6 CHANGE PN	0316	56, 57	1. PC187, PC190, PC192, PC200, PC201 改 C71-331037E-P01	0425	68	1. MA2 CHANGE FOOTPRINT
0309	69	1. CHANGE LED PN	0318	30	1. CHANGE 1V8MAIN & 3V3 SEQUENCE 2. ADD NVVDDS_PG DELAY CIRCUIT		63	1. MH13 CHANGE FOOTPRINT
	32	1. R159 STUFF AND PU CHANGE TO PD		31	1. ADD 3V3_AON DISCHARGE CIRCUIT, ADD R559	0506	31	1. R253, R240 STUFF AND PU CHANGE TO 1V8_AON 2. RSVD R367
0311	37	1. ADD R241, Q40	0322	35	1. U30 CHANGE TO BIOS PN, REMOVE BIOS1		25	1. R41 NO STUFF
	43	1. CHANGE PWR LED CIRCUIT , REMOVE Q16	0325	30	1. ADD 1V8MAIN_EN DELAY CIRCUIT		30	1. REMOVE R388 1. ADD U63, C1038 (STUFF) , R552, R551 (NOSTUFF) G1 CHANGE PN
			0330	45 67	1. OUT_R 6dB->10dB 2. OUT_L 6dB->10dB ONLY FOR 16K2	0509	60, 61	1. REMOVE PC214~PC220 1. PR142 1Kohm 2. PR145 3.3Kohm
							63	1. REMOVE UME4, UME6, UME8
						0512	70	1. REMOVE UMEC1

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